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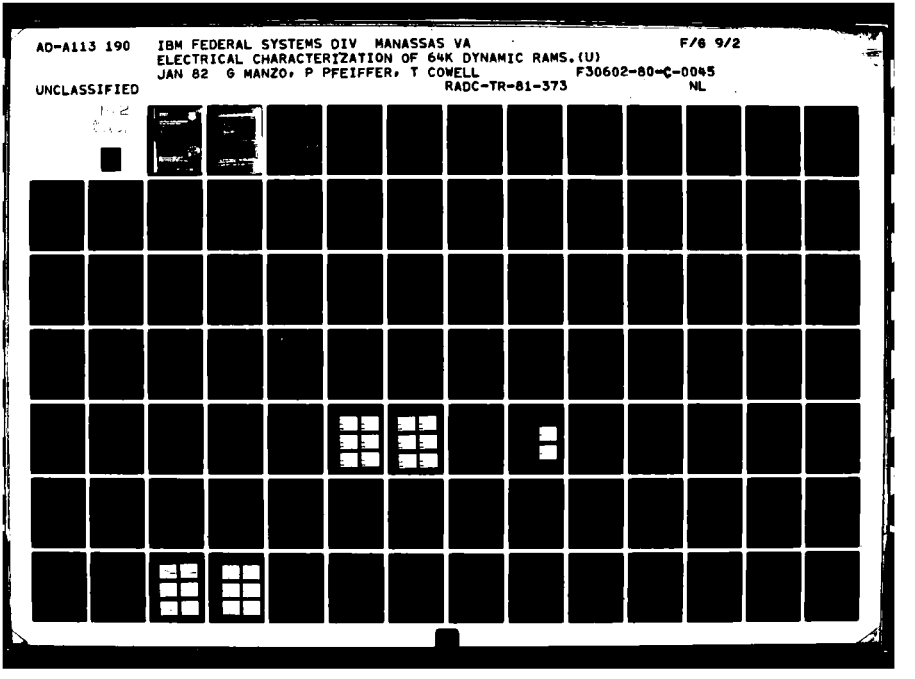

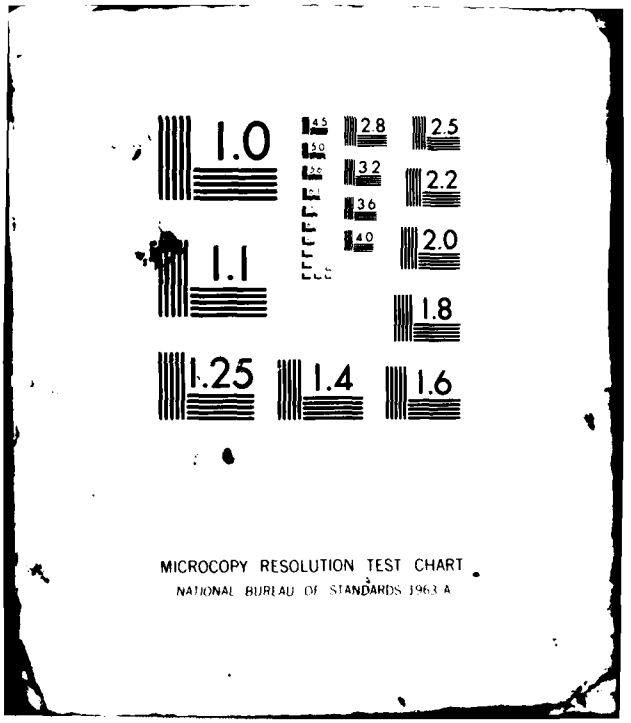
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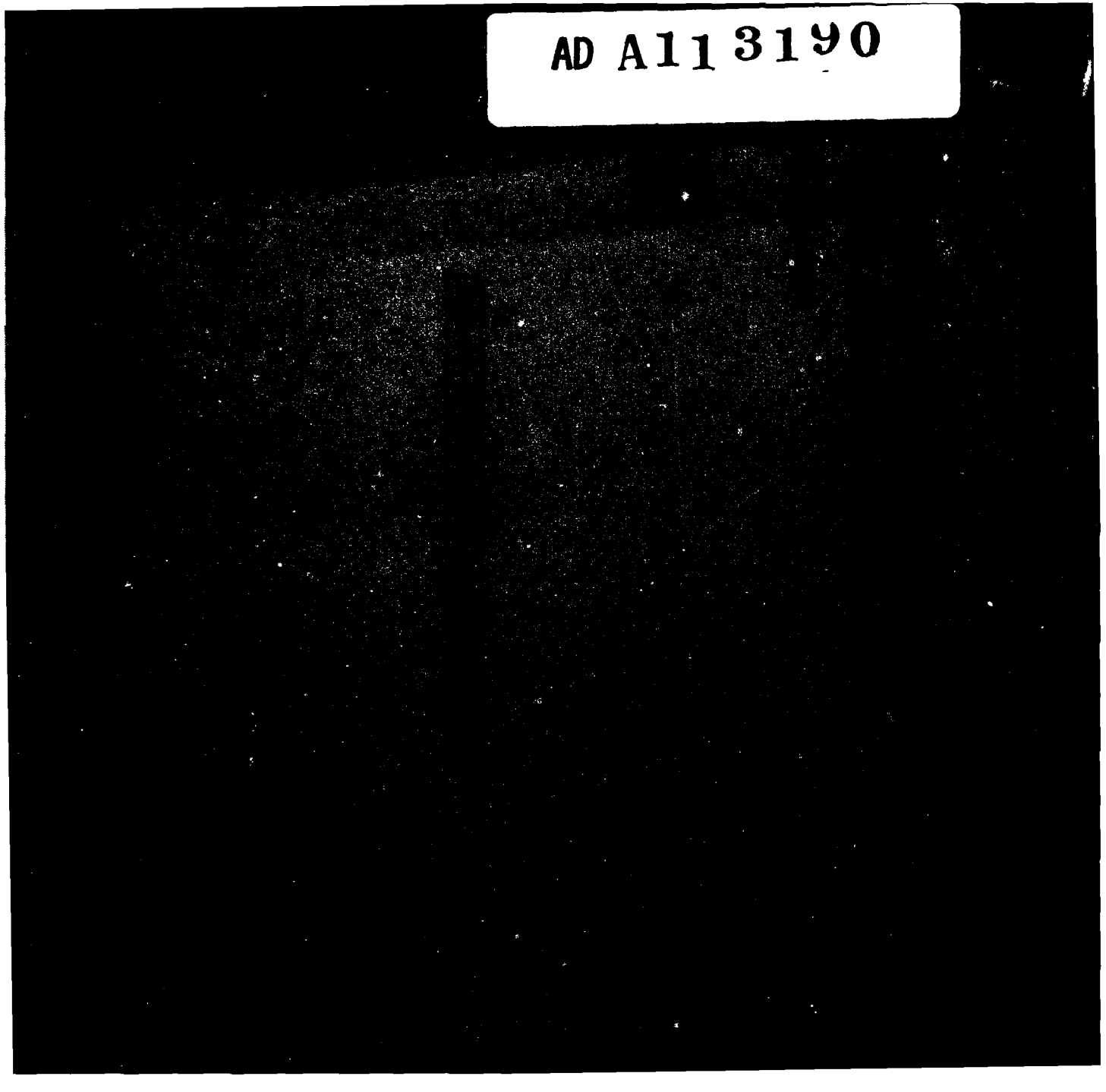

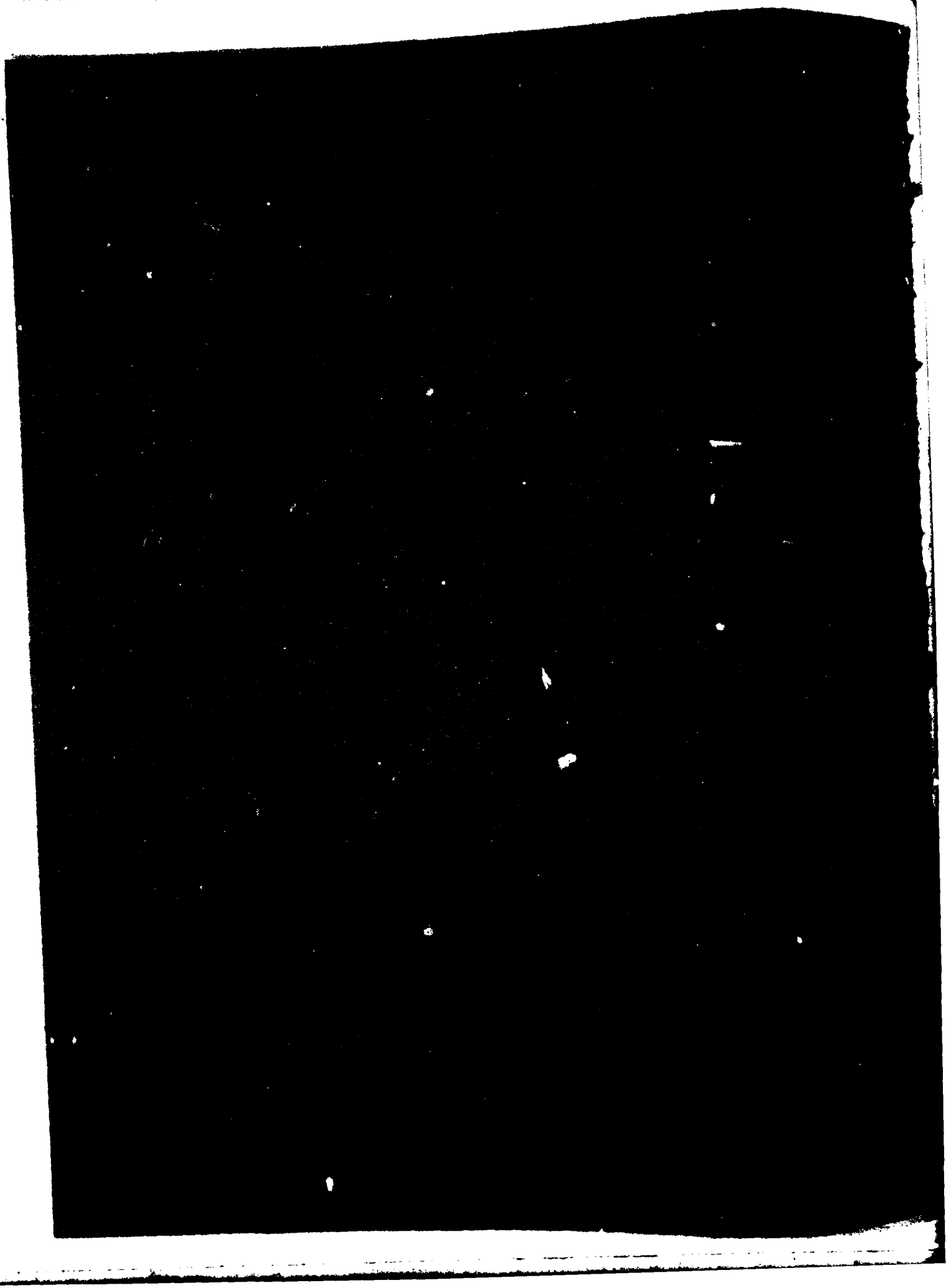

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Electrical characterizations were performed on 64K dynamic RAMs available from the merchant semiconductor industry. Based on the data obtained, parameter limits were established and proposed for the draft MIL-M-38510/244 specification. The data, proposed limits, and related discussion are presented. —> to pg iii

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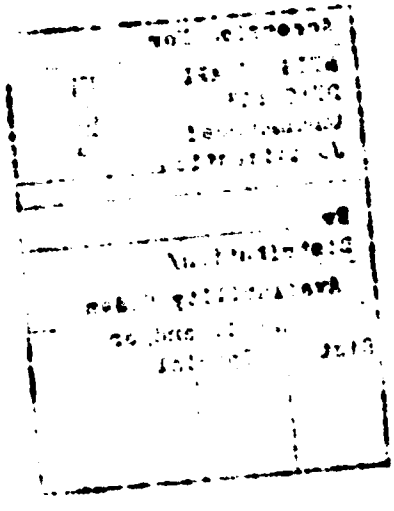
Evaluation

The objective of this program was to electrically characterize a representative sample of 64K Dynamic RAMs to establish their performance in a military environment. Based on this characterization, performance limits were to be established and incorporated into a draft MIL-M-38510 detail specification. IBM's approach to this task was extremely comprehensive, and because of their close working relationship with merchant vendors, they were able to select and characterize those devices which have the highest probability of becoming military qualified products. As this report indicates, their characterization was very thorough, and the draft specification (M38510/244) which resulted was comprehensive, of a high quality and was ready for coordination.

Allen P. Converse

ALLEN P. CONVERSE

Project Engineer



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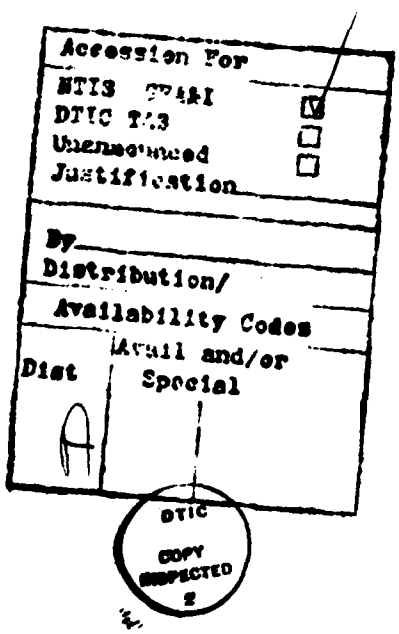

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Section 1

INTRODUCTION

The development of the 64K dynamic RAM has proven to be the most difficult task attempted by the merchant semiconductor industry to date. The requirement of a scaled NMOS technology with device geometries in the 2-3 micron range coupled with the decision to standardize on a single "5v only" device have resulted in an untold number of design and manufacturing problems and delays. The 64K development however has stimulated a multitude of design and process innovations and has finally reached volume production status. At this writing at least 15 merchant vendors will offer "unique" designs that contain many physical and functional differences.

The militarization of the previous generation 16K dynamic RAM has been successfully demonstrated (RADC-TR-79-5) and mutually accepted by both users and suppliers (MIL-M-38510/240). System sizings performed, utilizing the 64K dynamic RAM, have yielded outstanding cost, performance, ease of use, and reliability improvements when compared to systems implemented with 16K dynamic RAMs. For these reasons, which are shared by all military system suppliers, IBM Federal Systems Division (FSD) has performed electrical characterizations on 64K dynamic RAMs and generated a draft MIL-M-38510/244 military specification for the 64K dynamic RAM.

The final report is comprised of a large quantity of reduced data which justifies the limits set forth in the proposed draft specification. It is hoped that it will serve as a comparison reference manual for future product designs and revisions.

The explanation of the operation of the 64K dynamic RAM is covered in numerous data books, articles, and application notes and will not be repeated in this report.

Section 2

PROJECT OBJECTIVES

The objectives of the project were as follows:

1. Develop and refine a test philosophy for 64K dynamic RAMs that can be used for preparing a MIL-M-38510 detail specification.

2. Perform an electrical characterization over the military temperature range.

3. Attempt to demonstrate that devices made by different vendors are interchangeable on a pin and performance basis.

4. Generate a draft MIL-M-38510 slash sheet specification for the 64K dynamic RAM using characterization data as a basis for establishing performance limits.

Section 3

CONCLUSIONS

The objectives of this project were met in that 64K dynamic RAMs from four vendors were electrically characterized and a draft slash sheet, designated MIL-M-38510/244, was generated.

The slash sheet written reflects a 64Kx1 dynamic RAM implemented with 128 cycle refresh architecture and having pin #1 as a no-connect. Page mode was not included in this specification due to the added test time required and lack of user interest.

It has been concluded that the merchant semiconductor industry can supply 64K dynamic RAMs that will operate over the temperature range of $-55^{o}C$ case to $+110^{o}C$ case, with an access/cycle time of 150ns MAX/250ns MIN, a power supply tolerance of $\pm$10 percent, and a retention time of 1.0 MS minimum.

Shown in Tables 1 and 2 is a summary of the AC and DC parameter measurements at worst case conditions compared to the recommended slash sheet limits. For vendors A, C, and D the maximum (MAX) t_{RAC}, t_{CAC}, and t_{RC} values listed are close to or exceed the proposed limits. The average value (AVE) listed does however show that with proper screens, devices will meet the proposed limits. In addition, future and ongoing designs and processing tweaks are all aimed at improving these three key parameters. With this in mind, and noting that the devices tested were "off the shelf" commercial grade product, it is genuinely felt that the parameter limits listed in MIL-M-38510/244, with minor exceptions, will satisfy the majority of users and suppliers.

Included in MIL-M-38510/244 are recommended test algorithms and timing sets for screening parameter limits as shown in Appendix XII. Multiple passes through the memory are required to properly screen the parameter limits. The timing sets have been implemented and devices manufactured by different vendors have passed these timing conditions, thus proving device interchangeability on a pin and performance basis.

In addition, a soft error rate of 1 error per 10^6 device operating hours is required by MIL-M-38510/244. Suppliers are asked to perform a group C "system" soft error rate test to prove the integrity of their devices. Polyimide and silicone coatings are allowed as an overcoat on the die for alpha particle protection provided each lot is subjected to and passes group B, subgroup 1b tests. The internal moisture content after completion of all screening shall not exceed 5,000 ppm at $100^{\circ}C$. Restrictions were not placed on die coating thickness, cure time and temperature, application method, etc. These parameters will vary widely among the vendor designs. Accelerated soft error testing of 64K dynamic RAMs was performed and reported in IBM Federal Systems Division's Independent Research and Development Program (IR&D), Volume II, dated March 81.

Table 1. AC Characterization Data Overview at Worst Case (WC) Conditions

PARAMETER	SYMBOL	WC CONDITION V_{CC}/T_{CASE} (V/°C)	VENDOR A		VENDOR B		VENDOR C		VENDOR D		RADC
			AVE[2]	MAX[3]	AVE	MAX	AVE	MAX	AVE	MAX	PROP LIMIT
Random Read or Write Cycle Time	t_{RC}	4.5/110	242	248	198	208	220	230	228	236	250 MIN
Read Write Cycle Time	t_{RMW}	4.5/110	PASSED SCREEN AT 270 NS								270 MIN
Access Time from RAS	t_{RAC}	4.5/110	147	150	140	144	146	155	164	170	150 MAX
Access Time from CAS	t_{CAC}	4.5/110	72	75	85	88	85	90	99	103	90 MAX
Output buffer turn-off delay	t_{OFF}	4.5/110	PASSED SCREEN AT 0 NS								0 MIN
Output buffer turn-off delay	t_{OFF}	4.5/110	25*	-	30*	-	43*	-	47*	-	35 MAX
RAS precharge time	t_{RP}	4.5/110	79	85	43	50	59	68	49	53	90 MIN
RAS pulse width	t_{RAS}	4.5/110	139	145	122	125	100	110	143	148	150 MIN
RAS pulse width	t_{RAS}	4.5/110	PASSED SCREEN AT 10000 NS								10000 MAX
RAS hold time	t_{RSH}	4.5/110	79	85	43	50	59	68	49	53	90 MIN
CAS hold time	t_{CSH}	4.5/110	135	138	130	134	131	139	136	141	150 MIN
CAS pulse width	t_{CAS}	4.5/110	60	63	70	75	70	73	71	74	90 MIN
CAS pulse width	t_{CAS}	4.5/110	PASSED SCREEN AT 10000 NS								10000 MAX
RAS to CAS delay time	t_{RCD}	4.5/110	PASSED SCREEN AT 25 NS								25 MIN
RAS to CAS delay time	t_{RCD}	4.5/110	PASSED SCREEN AT 60 NS								60 MAX
CAS to RAS precharge time	t_{CRP}	4.5/110	PASSED SCREEN AT 0 NS								0 MIN
Row address set-up time	t_{ASR}	5.5/-55	-10	-9	-7	-6	-4	-4	-5	-4	0 MIN
Row address hold time	t_{RAH}	4.5/110	8	9	6	9	8	9	7	8	20 MIN
Column address set-up time	t_{ASC}	5.5/-55	-12	-11	-12	-10	-10	-9	-14	-14	-5 MIN
Column address hold time	t_{CAH}	4.5/110	11	12	12	15	13	15	23	25	30 MIN
Column address hold time referenced to RAS	t_{AR}	4.5/110	PASSED SCREEN AT 80 NS								80 MIN
Read Command set-up time	t_{RCS}	5.5/-55	-14	-14	-13	-13	-20	-18	-14	-14	0 MIN
Read Command hold time	t_{RCH}	5.5/-55	-6	-5	-15	-15	-6	-5	-12	-10	0 MIN
Read Command hold time referenced to RAS	t_{RRH}	5.5/-55	-6	-5	-15	-15	-6	-5	-12	-10	25 MIN
Write Command hold time	t_{WCH}	4.5/110	17	18	11	12	30	31	50	52	45 MIN
Write Command hold time referenced to RAS	t_{WCR}	4.5/110	83	86	63	66	75	78	112	117	120 MIN
Write Command pulse width	t_{WP}	4.5/110	5	5	6	7	11	12	14	15	45 MIN
Write Command to RAS lead time	t_{RWL}	4.5/110	10	11	24	25	18	20	44	47	45 MIN
Write Command to CAS lead time	t_{CWL}	4.5/110	12	13	24	26	15	16	35	36	45 MIN
Data in set-up time	t_{DS}	5.5/-55	-7	-6	-7	-7	-5	-5	-8	-8	0 MIN
Data in hold time	t_{DH}	4.5/110	14	15	10	11	19	20	44	46	45 MIN
Data in hold time referenced to RAS	t_{DHR}	4.5/110	81	84	62	66	63	66	110	114	120 MIN
Refresh Period (milliseconds)	t_{REF}	4.5/110	15	8	16	5	11	5	13	7	1.0 MIN
Write command set-up time	t_{WCS}	5.5/-55	-27	-24	-29	-27	-27	-25	-14	-13	0 MIN
CAS to WRITE delay	t_{CWD}	4.5/110	32	34	47	51	44	45	15	16	50 MIN
RAS to WRITE delay	t_{RWD}	4.5/110	105	105	104	105	103	110	81	85	110 MIN

NOTES: 1 - ALL PARAMETER VALUES ARE IN NANOSECONDS EXCEPT t_{REF} WHICH IS MILLISECONDS

2 - AVE IS AVERAGE VALUE FOR 15 UNITS AT WORST CASE CONDITIONS

3 - MAX IS MAXIMUM VALUE FOR 15 UNITS AT WORST CASE CONDITIONS

* - WORST CASE MEASUREMENT FOR A TYPICAL DEVICE

Table 2. DC Characterization Data Overview At Worst Case (WC) Conditions

PARAMETER	SYMBOL	WC CONDITION VCC/TCASE	VENDOR A		VENDOR B		VENDOR C		VENDOR D		RADC PROP LIMIT
			AVE[1]	MAX[2]	AVE	MAX	AVE	MAX	AVE	MAX	
Operating Current $\overline{RAS}$ $\overline{CAS}$ Cycling 250ns Cycle	I_{CC1}	5.5v/-55°C	54.4mA	56mA*	46.5mA	49mA*	41.7mA	43mA*	36mA	38mA*	60mA MAX
Standby Current $\overline{RAS}$ = $\overline{CAS}$ = VIH	I_{CC2}	5.5v/-55°C	3.6mA	4mA*	4.2mA*	4.5mA*	3.8mA	4.5mA*	4.0mA	4.5mA*	10mA MAX
Refresh Current $\overline{RAS}$ Cycling	I_{CC3}	5.5v/-55°C	40.5mA	42mA*	36.5mA	38mA*	31.4mA	32mA*	29mA	29mA*	45mA MAX
Input High Voltage	V_{IH}	5.5v/-55°C	-	>7.0v	-	>7.0v	-	>7.0v	-	>7.0v	6.5v MAX
$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ DIN			-	2.1v[5]	-	1.7v	-	1.9v	-	1.9v	2.4v MIN
Input High Voltage	V_{IH}	5.5v/-55°C	-	>7.0v	-	>7.0v	-	>7.0v	-	>7.0v	6.5v MAX
Addresses			-	1.9v	-	2.0v	-	2.1	-	2.1	2.4v MIN
Input Low Voltage	V_{IL}	4.5v/110°C	-	<-2.5v	-	<-2.5v	-	<-2.5v	-	<2.5v	-1.5v MIN
$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, DIN			-	1.1v	-	1.0v[4]	-	1.0v	-	1.1	0.8v MAX
Input Low Voltage	V_{IL}	4.5v/110°C	-	<-2.5v	-	<-2.5v	-	<-2.5v	-	<-2.5v	-1.5v min
Addresses			-	1.2v	-	1.3v[4]	-	1.4v	-	1.3	0.8v max
Input Leakage	$I_{I(L)(H)}$	N/A	SCREENED TO ±10μA								±10μA
Output Leakage	$I_{O(L)(H)}$	N/A	SCREENED TO ±10μA								±10μA
Output Source Current VOH=2.4v	I_{OH}	4.5v/110°C	-	-27mA	-	-15mA	-	-14mA	-	-12mA	-5mA MIN@ VOH=2.4v
Output Sink Current VOL=0.4v	I_{OL}	4.5v/110°C	-	25mA	-	22mA	-	14mA	-	7.1mA	4mA MIN@ VOL=0.4v
Input Capacitance A0-A7	C_{IN1}	N/A	-	4.7pF	-	3.3pF	-	4.6pF	-	4.3pF	5pF MAX
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, DIN, $\overline{WRITE}$	C_{IN2}	N/A	-	4.4pF	-	3.5pF	-	6.2pF	-	4.8pF	10pF MAX
Output Capacitance	C_{OUT}	N/A	-	4.1pF	-	5.0pF	-	5.4pF	-	4.7pF	8pF MAX

NOTES:
1. AVE is average of 15 units at worst case conditions
2. MAX is typical device worst case measurement
3. * denotes worst case of 15 units
4. Worst case at -55°C
5. Worst case at 110°C

Section 4

64K DYNAMIC RAM PROFILE

The previous generation 16K dynamic RAM evolved with very little variation. A standard approach was adopted by most all vendors. This approach consisted of 5μ double polysilicon process utilizing metal word lines, diffused bit lines and a storage capacitor tied to the V_{DD} (+12V) supply voltage.

The 64K dynamic RAM development has proven much different with every vendor pursuing their own innovative approach. This has resulted in many unique designs. Shown in Table 3 is a summary of the physical differences for 14 domestic and Japanese 64K RAMs. The entries, which consist of data accumulated over one year, are still changing as vendors optimize their designs.

A key difference noted in Table 3 is the number of sense amplifiers which is directly related to the refresh architecture. Dynamic RAM refreshing is accomplished by sensing and restoring the voltage levels present in each memory cell. This is done one row at a time. All 64K dynamic RAMs have a square matrix with 256 rows by 256 columns. Given 512 sense amplifiers the 256 rows are arranged as two sets of 128 rows and during every cycle (i.e. read, write or $\overline{RAS}$ only refresh) two rows are refreshed in parallel, thus only 128 cycles are required. With 256 sense amplifiers the number of required refresh cycles equals the number of rows (i.e. 256) since only one row can be refreshed at a time. Those designs utilizing 256 cycle refresh yield smaller die sizes and dissipate less power than 128 cycle devices.

Redundancy is also being employed on some vendor designs. In all cases spare rows and or columns replace defective rows and columns via electrically blown polysilicon fuses or laser blown links. This replacement is done at wafer sort and becomes transparent to the user. Redundancy can offer strong economic advantages in that the addition of spare rows, columns and logic adds only a small percent (<10%) to the overall die size but can result in a factor of 2 to 6 increase in yield during the early stages of production.

Table 3. 64K Dynamic RAM Technical Overview

	U.S. Vendors		Japanese Vendors	
	Range	Most Common	Range	Most Common
Vendors Surveyed	8	N/A	6	N/A
Die Size ($Kmils^2$)	34.5-51	<40[1] >40[2]	38-51	42
Data Matrices	2-8	4	2-8	4
Number of Sense Amplifiers	256/512	NOTE 3	512	512
Polysilicon Layers	1-3	2	2	2
Cell Size (μm^2)	131-195	∿170	152-198	∿195
Cell Capacitance (fF)	45-60	∿50	50-70	∿60
Cell to Bit Line Capacitance Ratio	1/11-1/15	∿1/15	1/8-1/12	∿1/9
Capacitor Plate	Grounded or Tied to V_{CC}	Tied to V_{CC}	Grounded or Tied to V_{CC}	Tied to V_{CC}
Bit Line Construction	Metal Poly-silicon Diffused	Metal	Diffused Metal	Diffused
Word Line Construction	Metal Poly-silicon	Poly-silicon	Metal Poly-silicon	Metal
Bootstrapped Wordline	No-Yes	Yes	No-Yes	Yes
Capacitor Oxide Thickness (Å)	375-700	∿400	350-600	∿400
Effective Channel Length (u)	2.3-2.8	∿2.4	2.4-3.0	∿2.5
Die Coating	Polyimide	Polyimide	Silicone Polyimide	Polyimide
Package (mils)	16 PIN DIP 18 PAD LCC[4] (295 x 435) and (295 X 475) 20 PAD LCC (295 x 435) 28 PAD LCC (350 x 550)		16 PIN DIP 18 PAD LCC (294 x 435)	

NOTES:
1. 256 Cycle Refresh Architecture
2. 128 Cycle Refresh Architecture
3. The eight US vendors surveyed are equally split with regard to the number of sense amplifiers.
4. LCC - Leadless chip carrier. The body size of the LCC is shown in parenthesis in mils.

Common to all 64K dynamic RAM suppliers are the design goals to maximize stored charge and increase sense amplifier discrimination. These goals are required to minimize alpha generated soft errors, and in part, have given rise to the large variation now found in the vendor designs. Some of the techniques used to realize these goals are briefly explained below:

Memory Cell Capacitance: There are at least 4 methods used to increase cell charge capacity. The first requires a larger capacitor area and thus a larger cell size. This method is somewhat undesirable since it results in a larger die and lower yield per wafer. A second method is to reduce the thickness of the storage capacitor oxide. This method has been extensively utilized in the design of 64Ks (i.e. 16K capacitor oxide thickness were $\sim$ 900Å). The third method is to use an insulator with a higher dielectric constant than SiO_2. To date all known 64Ks in production use SiO_2 as an insulator. However, one vendor has experimented with an alternate insulator to realize a 2x improvement in cell capacitance. The fourth method requires a P+ type implant beneath the N type silicon storage region to in effect form a reverse biased diode, which adds a depletion region component to the storage cell capacitance. This method referred to as a Hi-C cell has been implemented in some 64K designs. Additionally, novel cell designs (e.g. triple-polysilicon cell) may increase charge capacity for the same storage area.

Wordline Bootstrapping: This is a technique used to maintain the highest possible voltage level in the cell. Bootstrapping is performed by capacitively increasing the wordline potential to a voltage higher than the supply (typically 7v) and thus storing 7v (minus a device threshold) instead of the normal 5v (minus a device threshold).

Metal Bit Lines: In some designs metal bit lines have replaced diffused bit lines (used extensively on 16Ks) for two key reasons. First, implementing metal bit lines results in a smaller junction area within the silicon material and thus a smaller target for electron-hole pairs generated by an alpha hit. Secondly, replacing the diffused bit line with a metal bit line allows closer packing and/or larger capacitor plates since the metal bit lines are not in the same plane as the diffused bit lines and capacitor storage regions (i.e. metal bit lines are above the silicon region, whereas diffused bit lines and capacitor storage regions are in the silicon and adjacent to each other).

Folded Bit Lines: This is a layout technique whereby the two bit-sense lines feeding the sense amplifier are physically adjacent to each other. In this configuration noise (e.g. alpha particle) is coupled to both lines and in effect cancelled, allowing proper sense amplifier discrimination.

Substrate Resistivity: To guard against peripheral circuit noise (and again alpha particle hits) it is best to have a low resistivity substrate. This coupled with short diffusion lengths would allow electron-hole recombination before disturbing the storage cells. However the trend is to implement high resistivity substrates in dynamic RAMs to reduce junction capacitance. A possible solution as implemented by one 64K RAM supplier, is to deposit an epitaxial layer of high resistivity P- silicon onto a low resistivity P+ substrate.

Capacitor Plate Reference: The capacitor plate in the 16K dynamic RAM was initially tied to the unregulated V_{DD} (+12v) supply. A test, called V_{BUMP}, was developed for the 16K RAM to determine sense amplifier margin. This test is performed by varying the V_{DD} supply, which in turn modulates the cell voltage via the capacitor plate. The amount of allowable cell voltage change (i.e., before failure) can be used to measure the margin at the sense amplifier. To eliminate cell voltage changes due to variations in the supply voltage, 64K designs follow one of two approaches. The capacitor plate is grounded and a N+ implant is placed beneath the capacitor plate for diffusion store, or the capacitor plate is tied to a regulated V_{CC} (+5v) supply and the cell relies on inversion layer storage.

Die Coat: At the present time, all manufacturers of 64K dynamic RAMs have elected to use die coatings to improve their products' soft error rate due to alpha particles. Two materials (silicone and polyimide) are being employed. These coatings prevent alpha particles from penetrating the die surfaces by absorbing these particles. Polyimide coating thickness typically range from 0.7 to 3 mils whereas, silicone coatings are 4 to 25 mils thick.

Finally, with regard to dynamic RAM processing, most vendors use direct step-on-wafer photolithography, dry plasma etching and E-Beam generated masks. Some vendor designs utilize multiple threshold devices and thus extra processing steps are needed.

Section 5

CHARACTERIZATION APPROACH

5.1 SAMPLE SELECTION

The philosophy established at the outset of the project was to arrive at a set of specification limits that are both attractive to a user and deliverable by the industry with little added in the way of special electrical tests. Rather than testing a large number of samples from a single vendor, data was collected on a lesser number of devices representing several suppliers. This philosophy was chosen considering the frequent number of design iterations occurring during the span of the project and also to demonstrate multiple sourceability to the proposed specification limits.

The characterization sample set included fifteen devices each of four manufacturers (two domestic and two Japanese) currently shipping 64K RAMs in production quantities. The Japanese vendors, chosen due to the maturity of their designs, are potential long term JAN suppliers since both are planning to manufacture 64K RAMs in U.S. based facilities. A single device from vendor D was destroyed during early testing and therefore only fourteen devices from this vendor are included in all data.

One of the domestic suppliers selected utilizes a 256 cycle refresh architecture as opposed to the 128 cycle architecture of the remaining vendors devices. All devices were procured as "off the shelf", 150NS access time, commercial temperature range devices packaged in 16 pin ceramic Dual-Inline Packages.

While several Pin #1 refresh functions have been developed by 64K RAM designers, consistency has not been maintained throughout the industry. This together with the fact the 256K RAM will use pin 1 as an address input limiting upward compatibility from the 64K, led to the decision to characterize devices with pin 1 as a no-connect.

5.2 TEMPERATURE RATIONALE

In the dynamic RAM cell, data is stored as charge on a capacitor. Stored data will degrade with time and increased temperature. The dependancy of retention time to increased temperature is exponential (i.e. a small increase in temperature results in a fairly large decrease in cell charge). Since stored charge determines the integrity of the RAM cell, the upper temperature limit is a key concern to the military dynamic RAM designer. The 16K dynamic RAM (Mil-M-38510/240) set the precedent for having an upper limit of 110°C case (not ambient). This has been accepted by both users and suppliers. The 64K dynamic RAM will be consistent with the 16K RAM and have an operating temperature range of -55°C to +110°C case. The corresponding refresh interval is discussed in Section 6.6.

Two temperature forcing systems were used providing a controlled case temperature environment of -55°C to +110°C. The primary system was a Thermonics (Model T-2050) forced nitrogen unit used for the bulk of the AC characterization. A Temptronic hot probe (Model TP 26/27) and cold probe (Model TP27C) were used for oscillograph and cell retention measurements. In each case a Digitec (Model 590TC type T) Thermocouple thermometer was centered between the device under test and the DIP socket used while exercising the memory. Thermocouple temperatures of -55°C, +25°C and +110°C were maintained throughout the testing period.

5.3 MEMORY TEST EQUIPMENT

A Fairchild Xincom 5582 Memory Test System was used for all AC testing. An extensive characterization software set was developed for the programmable tester providing accurate measurement of both AC and DC parameters. In addition to single point measurement data the Xincom also provides 2-dimensional and 3-dimensional schmoo plots, histograms and V_{BUMP}/V_{BOBBLE} test data.

Section 6

CHARACTERIZATION PROCEDURE/DATA DISCUSSION

6.1 AC PARAMETERS

Parameter listing data taken on the Xincom tester was compiled on all 59 devices at -55°C, 25°C, and 110°C case temperature. This data consists of 39 AC parameter measurements performed with V_{CC} equal to 4.5v, 5.0v, and 5.5v. The AC data was taken using a March addressing/data pattern and "loose" timing. For each parameter a software subroutine was written that would seek out the exact pass/fail point for that parameter. An example of a measurement routine and timing is shown in Figure 1.

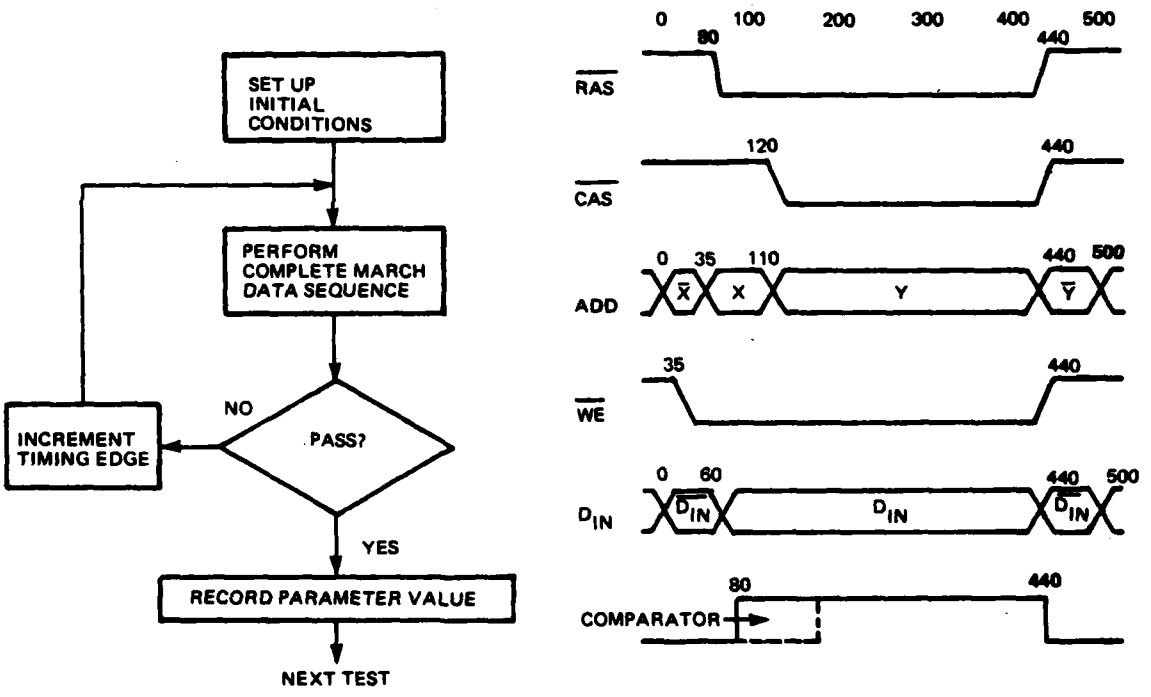


Figure 1. AC Measurement Test Flow and Timing Example

All AC data was taken with address and clock V_{IH} and V_{IL} of 2.4v and 0.8v respectively. Data out comparator levels were set to V_{OH} = 2.4v and V_{OL} = 0.4v with 100 pF capacitive load to V_{SS}.

Reduction of the AC listing data, performed using APL, is presented in Appendix I. Each parameter is plotted as a function of case temperature and as a function of supply voltage. Each curve contains three measured data points which have been fit to a second-order polynomial equation as are all plotted data in this report. The eight curves on each graph represent the worst case device at worst case conditions (V_{CC} or T_{CASE}) and average of 15 devices at nominal conditions, for each of the four vendors.

A summary of the AC parameter data is discussed in Section 3.

6.2 SUPPLY CURRENT

Supply current measurements were performed with cycle times of 250NS, 500NS, and 10000NS for the 9 case temperature/supply voltage combinations. This data, presented in Appendix II, is shown as a function of voltage, temperature, and cycle time. Each graph represents the worst case device for each vendor and is plotted for a random read/write cycle, a $\overline{RAS}$-only cycle, and in standby mode. Average or typical curves are not shown due to the tight distribution of this parameter as indicated by the I_{CC} histograms. All supply current measurements were made on the Xincom tester.

Results of supply current measurements indicate all devices met the proposed specification limits of 60mA, 45mA, and 10mA for active, refresh, and standby current respectively. At worst case conditions of -55°C and 5.5v maximum active I_{CC} ranged from 36mA to 56mA for the 59 devices.

Appendix II also contains oscillographs of V_{CC} supply transient currents taken at +110°C, 25°C, and -55°C case temperature at V_{CC} = 5.5v on a typical device from each vendor. A 250NS read cycle timing set was used with $\overline{RAS}$ positioned for 150NS minimum t_{RAS}. The photographs are double exposures with the upper current trace illustrating a random read/write cycle and the lower trace illustrating a $\overline{RAS}$-only cycle. This data was taken using a Tektronix CT-2 current transformer connected at the V_{CC} pin.

Peak transient current and maximum $^{di}/_{dt}$ observed in this data were 163mA and approximately 10mA/NS at -55°C and 5.5v.

6.3 SUBSTRATE CHARACTERISTICS

Three types of data relating to the negatively biased substrate and substrate bias generator are presented in Appendix III. These are (1) oscillographs of substrate bias generator turn-on time, (2) static measurements of substrate voltage as a function of temperature and supply voltage, and (3) schmoo plots of access time vs. forced substrate voltage vs. supply voltage. Vendors C & D were not included in the study since the substrate was not accessible (or not negatively biased).

The triple exposure oscillographs show the substrate bias generator turn-on time at -55°C, 25°C, and +110°C. A 100µs pause is required after V_{CC} is applied to allow sufficient time for the substrate to reach an adequate negative potential. By combining the substrate voltage measurement data with the schmoo data at each temperature, a relative indication of operating margin can be obtained. In each case adequate margin was demonstrated in the 4.5v to 5.5v supply voltage range.

6.4 BUMP VOLTAGE SCHMOO (V_{CC} SLEW TEST)

Schmoo data of V_{CC} during a write cycle vs. V_{CC} during a read cycle (V_{BUMP}) is presented in Appendix IV for a typical device from each vendor at -55°C, 25°C, and +110°C. This test, performed using loose timing and the functional pattern described in Appendix XII, is indicative of sense amplifier discrimination. The 10 percent supply minimum operating window, drawn on each schmoo, shows "bumping" from a low V_{CC} during write to high V_{CC} during read at -55°C to be worst case. While vendors A and C demonstrated good margin and vendor B only failed at the single worse case point at -55°C, vendor D did not pass the entire window at any temperature.

6.5 $\overline{RAS}$ TO $\overline{CAS}$ DELAY SCHMOO

A three dimensional schmoo plot of access time from $\overline{RAS}$ vs $\overline{RAS}$ to $\overline{CAS}$ delay vs supply voltage was taken for a typical speed device from each vendor at -55°C and 110°C. Analyzing this data, one can determine (1) t_{RAC} vs V_{CC}, (2) t_{CAC} vs V_{CC}, (3) t_{RCD} (max) vs V_{CC}, and (4) t_{RCD} (min) vs V_{CC} (or gated $\overline{CAS}$.) This data is presented in Appendix V.

6.6 CELL RETENTION

Data retention time was measured for each of the 59 devices at 110°C. The average for each vendor is presented in the parameter comparison table in Section 3. The worst case, and a typical device from each vendor are plotted as a function of temperature in Appendix VI. A pattern similar to pattern 8 (Appendix XII) was used performing a burst refresh at the measured interval. Temperature measurement points of 95°C, 110°C, and 125°C were used with V_{CC} = 4.5v. Every device performed within the 1 MS proposed specification, with averages between 5 and 9 MS. This represents a significant improvement over earlier devices audited during this study which in some cases only marginally met the 1 MS goal.

6.7 HISTOGRAMS

For the purpose of illustrating the relative distribution of key parameters among the 59 devices evaluated, histogram data of t_{RAC}, t_{CAC}, t_{RC}, t_{RP}, and I_{CC1} is presented in Appendix VII. Data on the four AC parameters was taken at V_{CC} = 4.5v, while I_{CC} data was taken at V_{CC} = 5.5v, and t_{RC} = 250NS. Detailed measurements for these parameters are shown in Appendix I. In general, all vendors maintained a fairly tight distribution for operating current measurements. For the AC parameters, vendors A and B again maintained a tight distribution whereas, C and D exhibited a 24NS and 20NS spread respectively, at 110°C for t_{RAC}.

6.8 OUTPUT TURN-OFF DELAY

Data output turn-off delay as a function of case temperature, supply voltage, and capacitive load is presented in Appendix VIII in the form of triple exposure oscillographs. Appendix XII pattern 2 describes the measurement criteria and procedure used for this data. Figure 2 displays the output load circuit that was used for all t_{OFF} data.

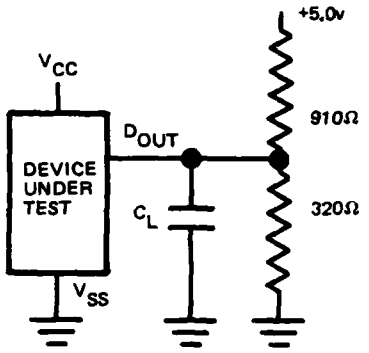


Figure 2. Output Turn-Off Delay (t_{OFF}) Load Circuit

Results of the t_{OFF} data indicate that only vendors A and B meet the 35NS maximum proposed specification. The failing transition for vendors C and D, which is evident from the photographs, is the disable from a "0", taking in excess of 40NS for the two devices.

6.9 INPUT LEVEL SENSITIVITY

Address and clock input level schmoo data as a function of V_{CC} was taken on a typical device from each vendor at -55°C, 25°C, and +110°C case temperature. This data was reduced and is plotted as a function of supply voltage and temperature in Appendix IX. Loose timing was used as was a March addressing/data pattern for all input level data. Although the plotted data only shows minimum V_{IH} and maximum V_{IL}, data was also taken verifying operation to V_{IH} (max) = 7.0v and V_{IL} (min) = -2.5v for all vendors.

6.10 OUTPUT SOURCE AND SINK CURRENT

Presented in Appendix X are output source, sink, and short circuit current measurements as a function of case temperature and supply voltage. A typical device was selected and characterized at the 9 voltage/temperature combinations. Data was taken on an analog XY plotter providing a continuous plot of I_{OUT} for V_{OUT} from 0v to 7v. The test circuit and timing used is also shown in Appendix X. Extracted from these plots is I_{OH} at V_{OH} = 2.4v, I_{OL} at V_{OL} = 0.4v, and I_{OS} at V_{OH} = 0.0v. At worst case conditions of 110°C and 4.5v, a minimum I_{OH} of 12mA and

minimum I_{OL} of 7 mA was measured. I_{OS} for all devices ranged from 45 mA to 199 mA. Vendor A exceeded the proposed absolute maximum rating for I_{OS} at -55°C.

6.11 DEVICE CAPACITANCE

Presented in Appendix XI are device input and output capacitance measurements taken with a BOONTON Model 72BD capacitance meter. The meter uses a test frequency of 1 Mhz. Measurements were made with V_{CC} = 5.00v and taken under biased conditions. Increasing the bias from 0v to 2.4v in the case of the clock inputs, increases capacitance by 0.2 to 2.5 pf. The worst case reading for each input and the data output pin are presented. All measurements were within the 5pF, 10pF, and 8pF proposed limits for address inputs, clock inputs, and output capacitance respectively.

6.12 PATTERN SENSITIVITY

The change in access time due to address sequence was investigated by taking schmoo data of t_{RAC} vs supply voltage using four addressing patterns. The patterns used were (1) March Data (Appendix XII pattern 6), (2) Sequential read/write, (3) Address Complement (Appendix XII, pattern 4), and (4) Galloping Row/Column. The galloping row/column pattern performs $N^{3/2}$ cycles/pass through the array and was used rather than the lengthy Galpat (N^2) due to the impractical time required for a Galpat schmoo. Since pure topological addressing is required, bit maps were obtained from vendors A and B and loaded into the Xincom tester. Complete bit maps from vendor C and D were not available. Results of this data show a 2NS or less variance in access time for the patterns used.

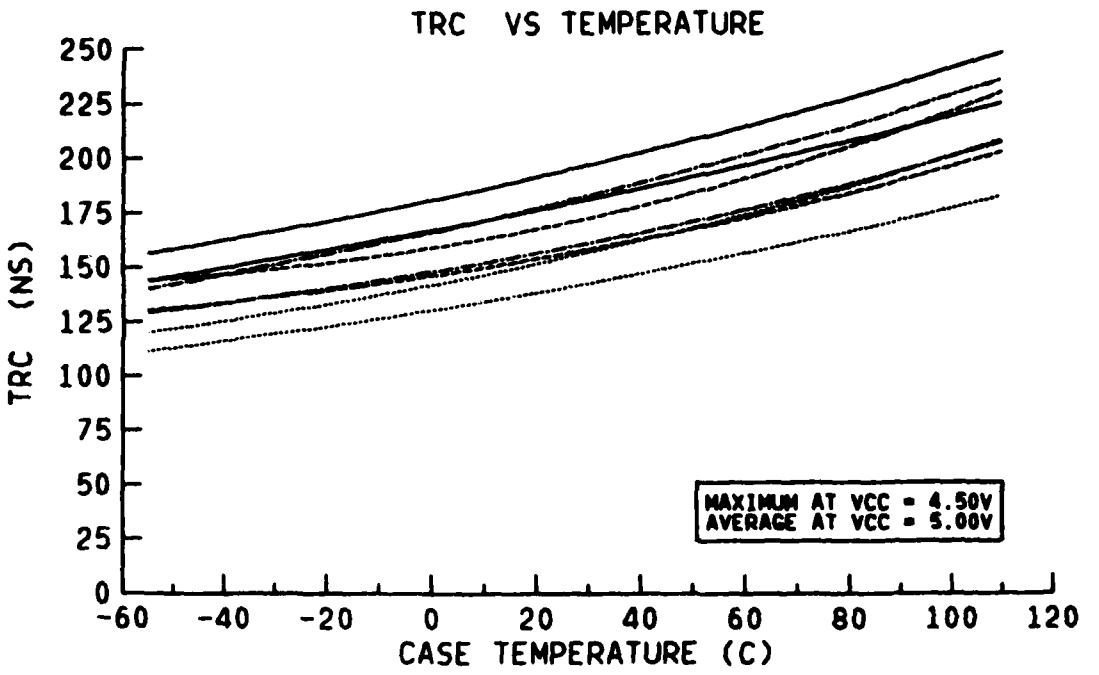
APPENDIX I

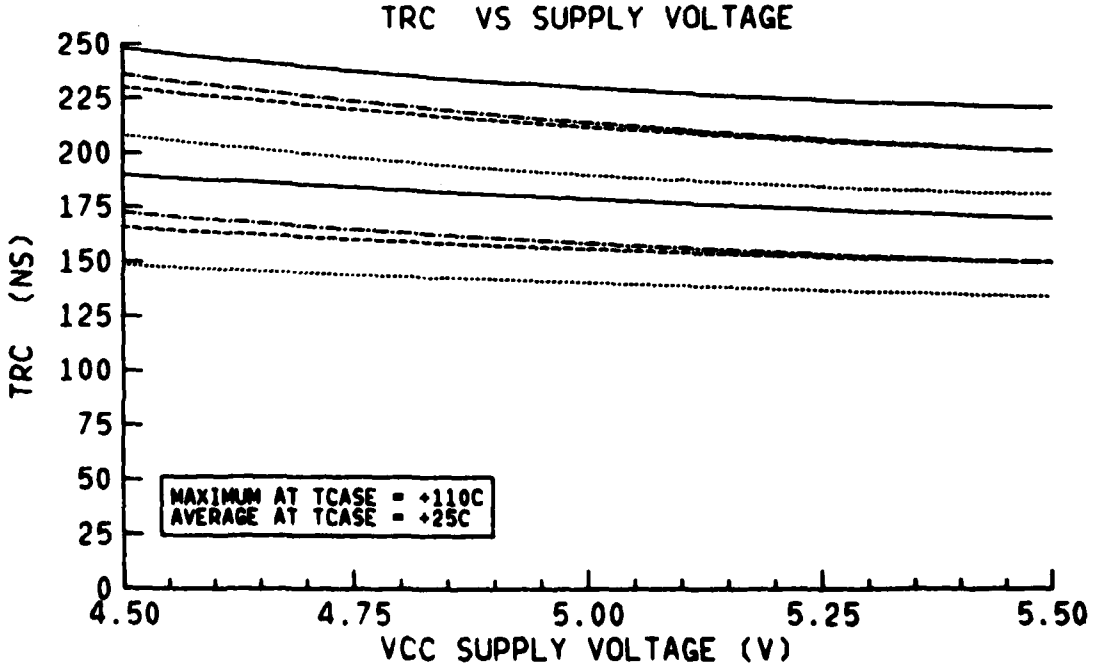
AC PARAMETER GRAPHS

VENDOR A
VENDOR B
VENDOR C
VENDOR D

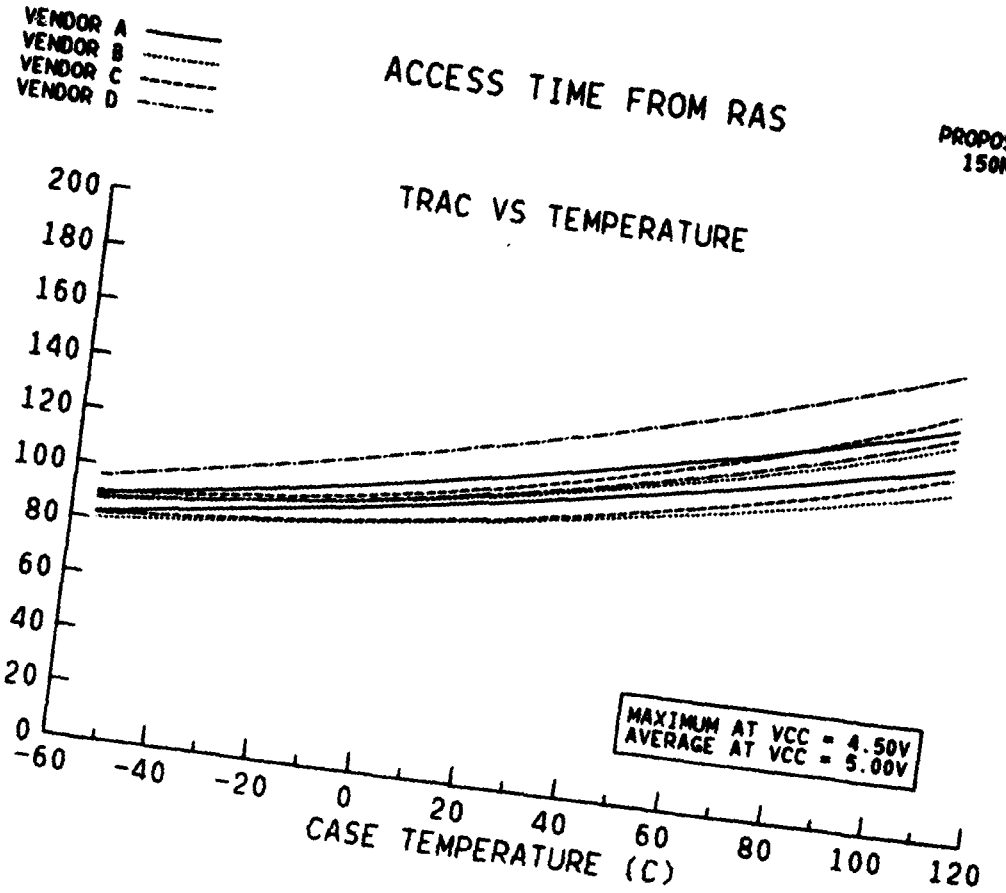
RANDOM READ OR WRITE CYCLE TIME

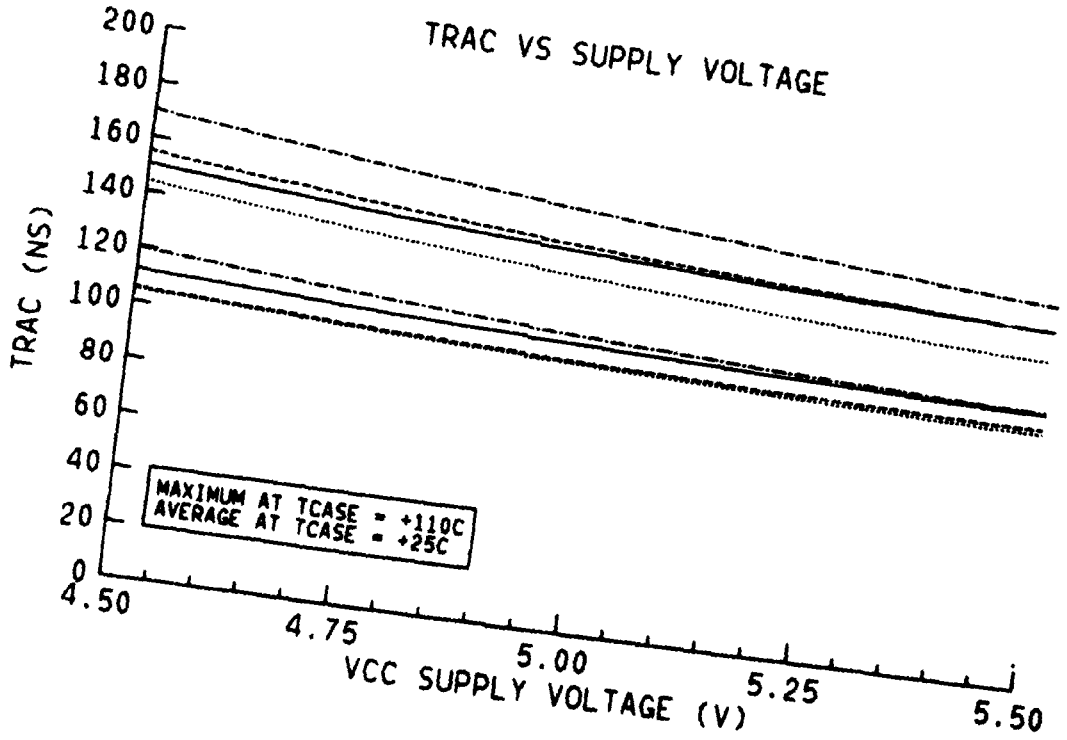
PROPOSED LIMIT
250NS MIN





ACCESS TIME FROM RAS



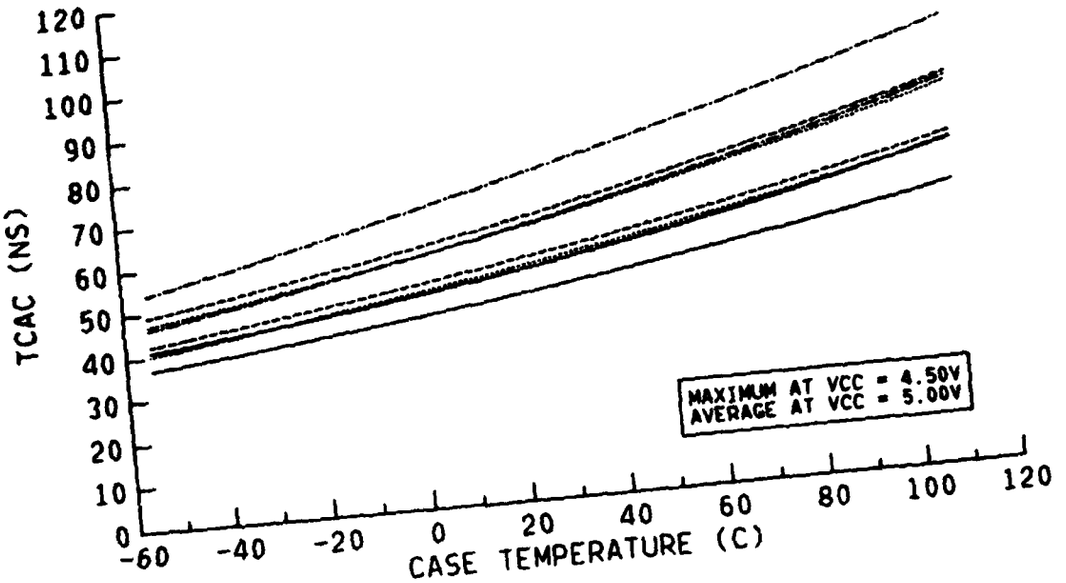


ACCESS TIME FROM CAS

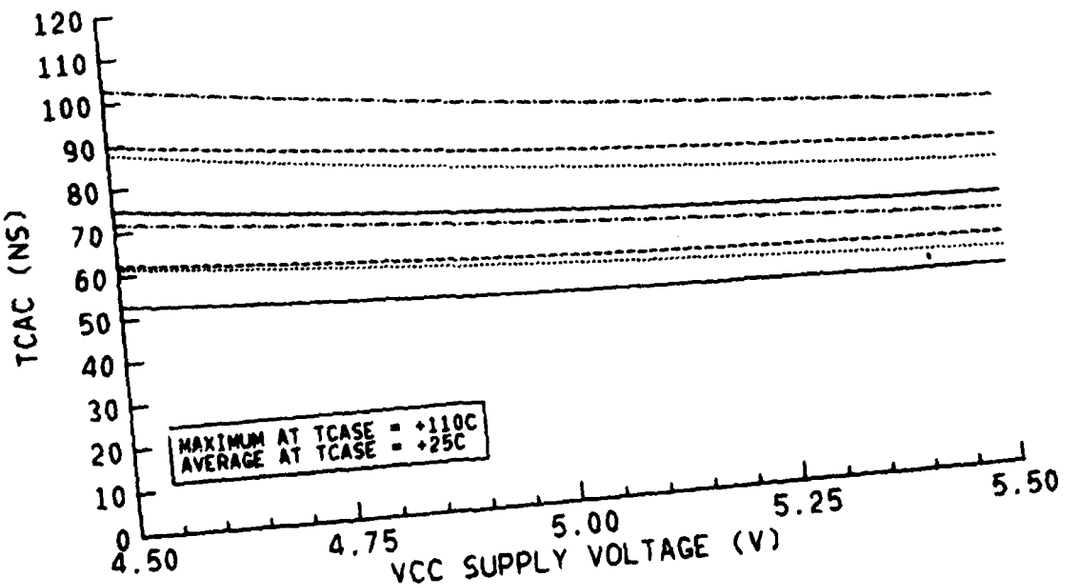
PROPOSED LIMIT
90NS MAX

VENDOR A
VENDOR B
VENDOR C
VENDOR D

TCAC VS TEMPERATURE



TCAC VS SUPPLY VOLTAGE

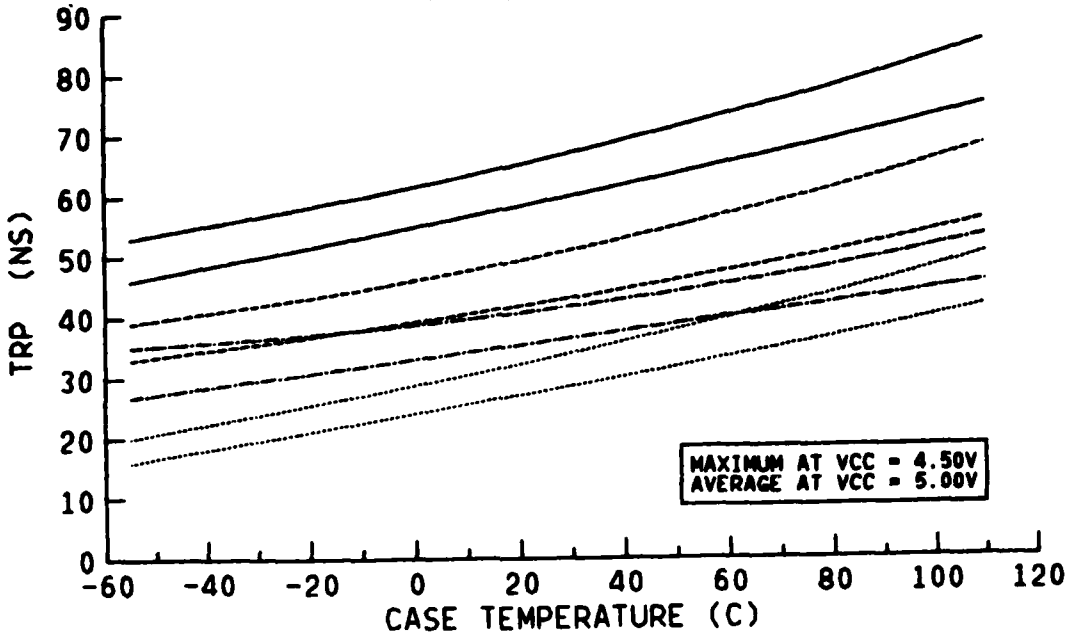


VENDOR A
VENDOR B
VENDOR C
VENDOR D

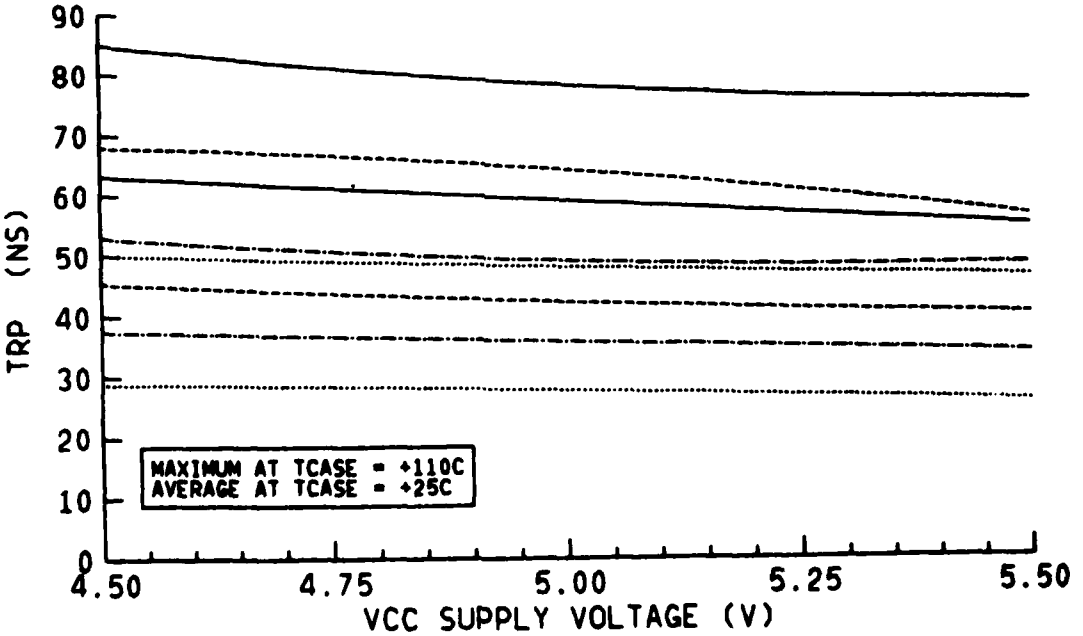
RAS PRECHARGE TIME

PROPOSED LIMIT
90NS MIN

TRP VS TEMPERATURE



TRP VS SUPPLY VOLTAGE

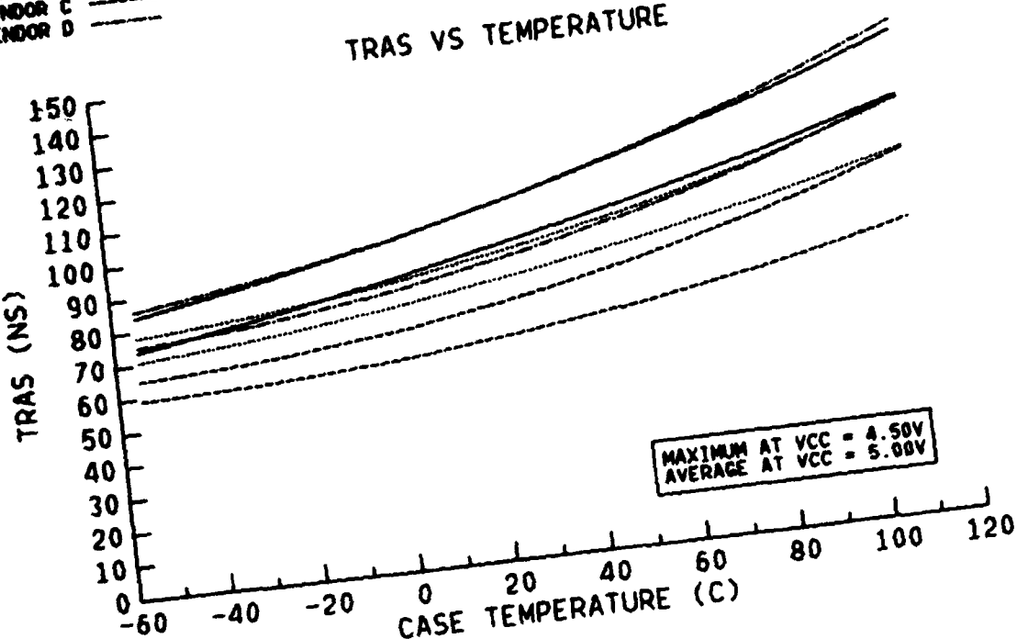


RAS PULSE WIDTH

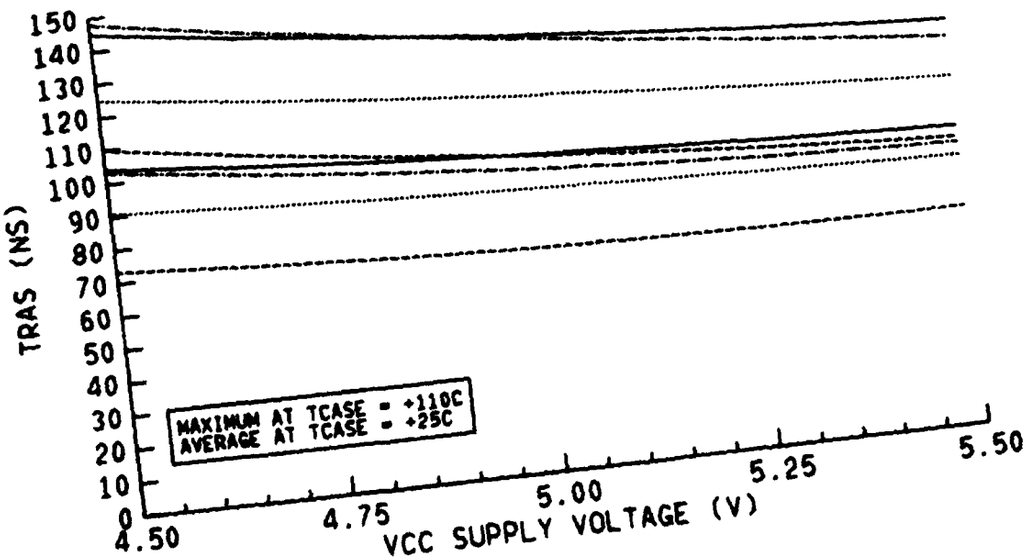
PROPOSED LIMIT
150NS MIN

VENDOR A
VENDOR B
VENDOR C
VENDOR D

TRAS VS TEMPERATURE



TRAS VS SUPPLY VOLTAGE

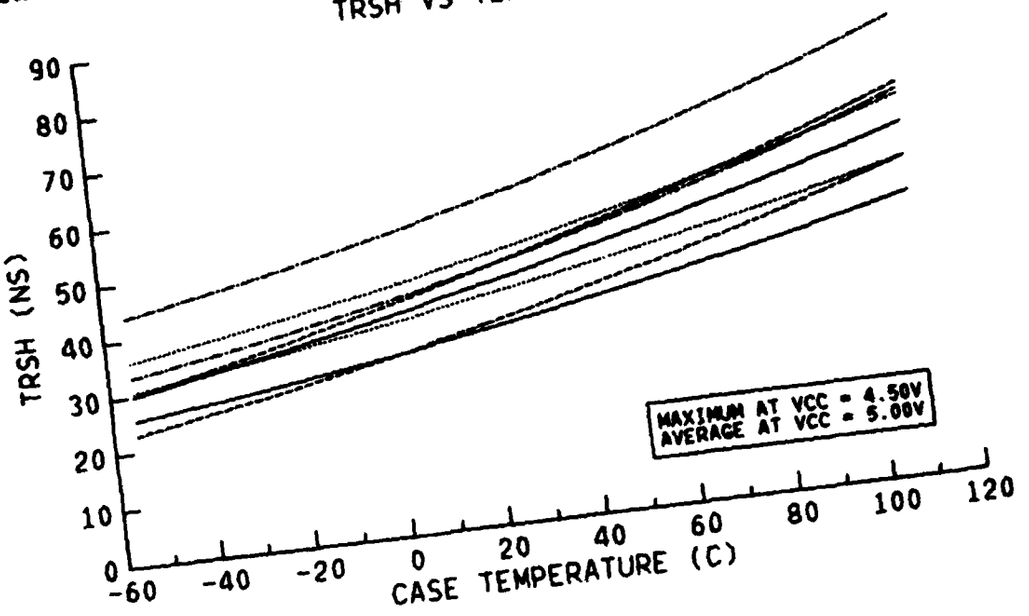


RAS HOLD TIME

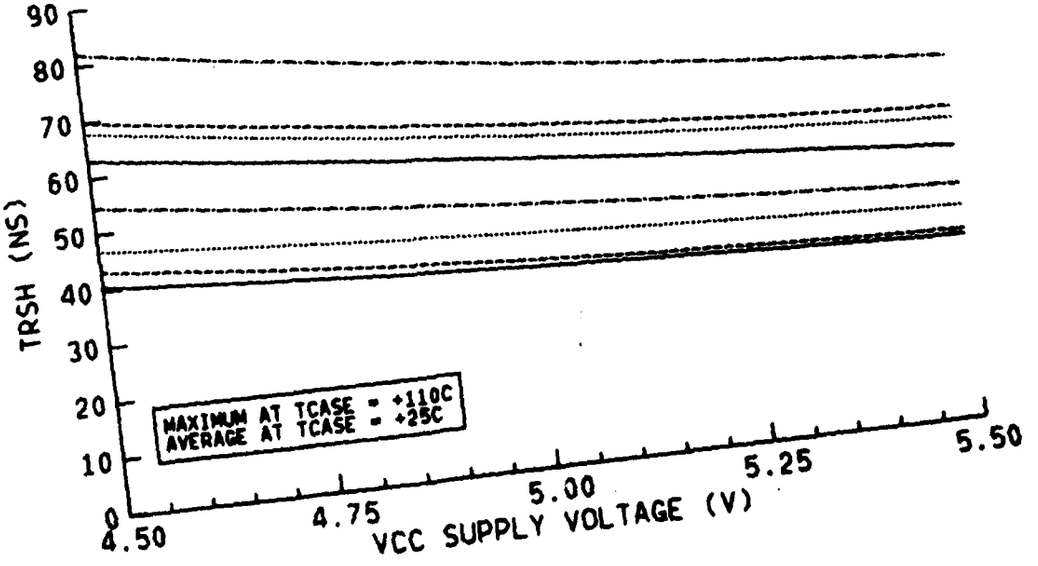
PROPOSED LIMIT
90NS MIN

VENDOR A
VENDOR B
VENDOR C
VENDOR D

TRSH VS TEMPERATURE



TRSH VS SUPPLY VOLTAGE

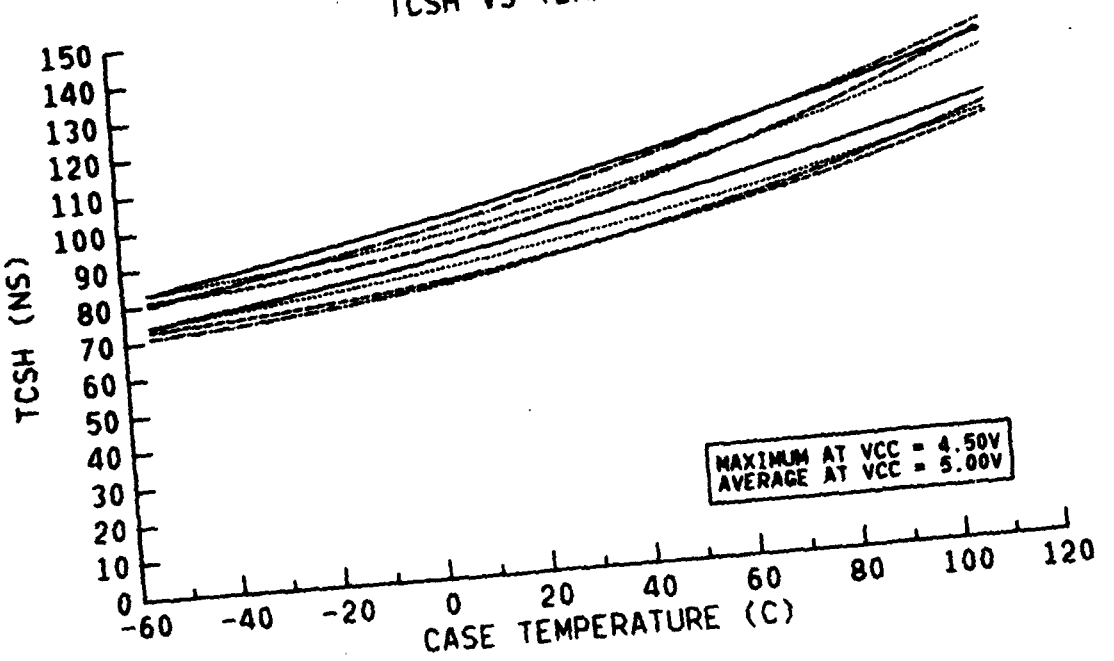


CAS HOLD TIME

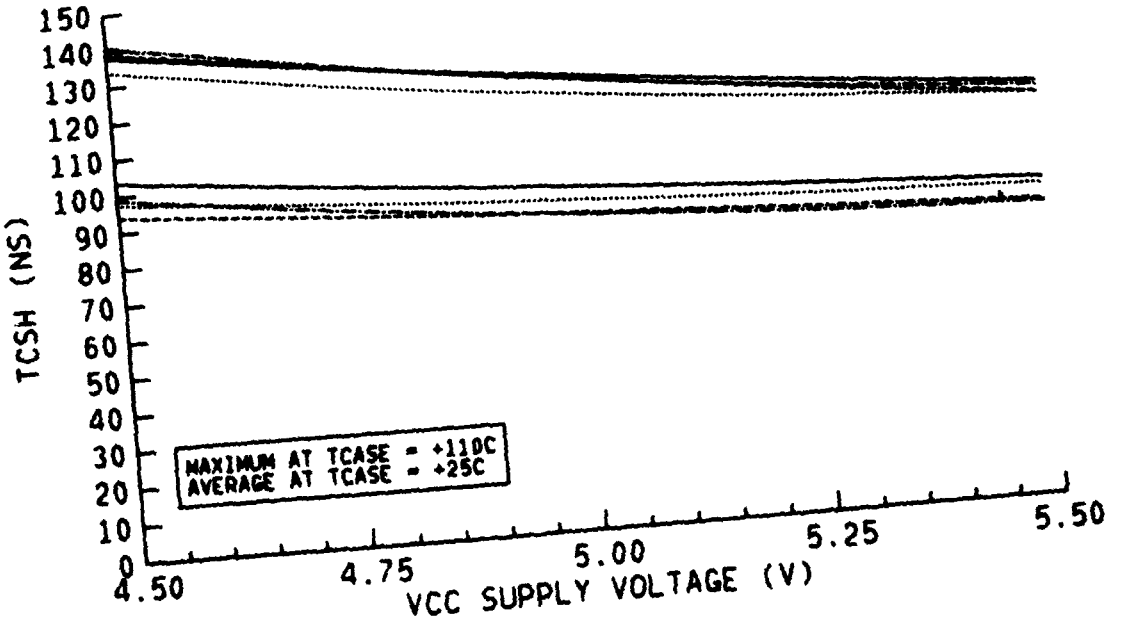
PROPOSED LIMIT
150NS MIN

VENDOR A
VENDOR B
VENDOR C
VENDOR D

TCSH VS TEMPERATURE



TCSH VS SUPPLY VOLTAGE

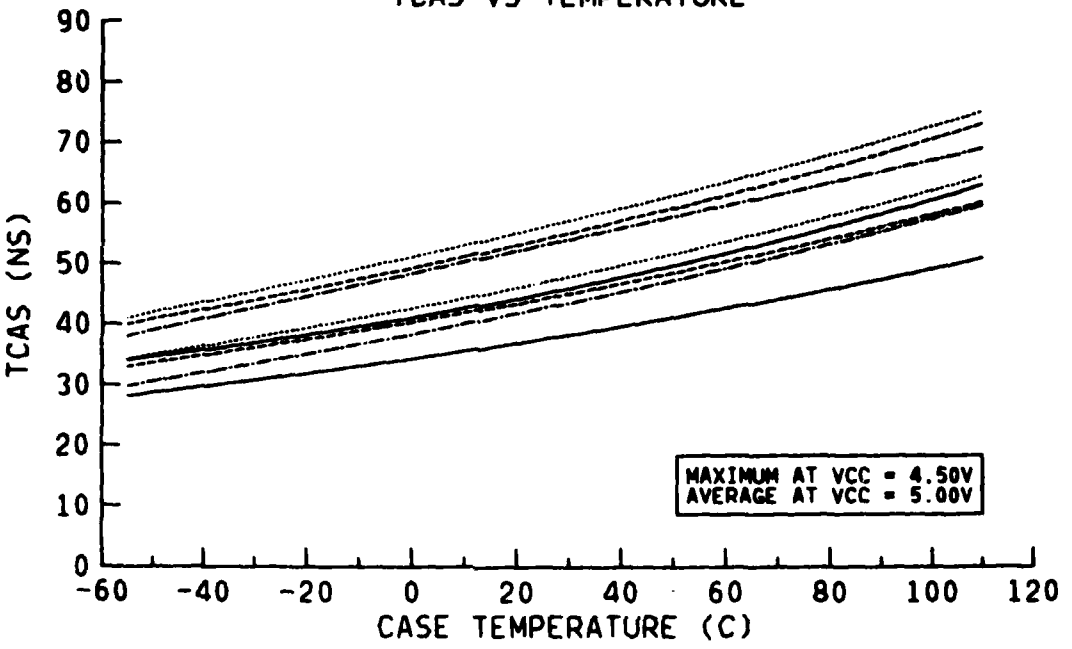


VENDOR A
VENDOR B
VENDOR C
VENDOR D

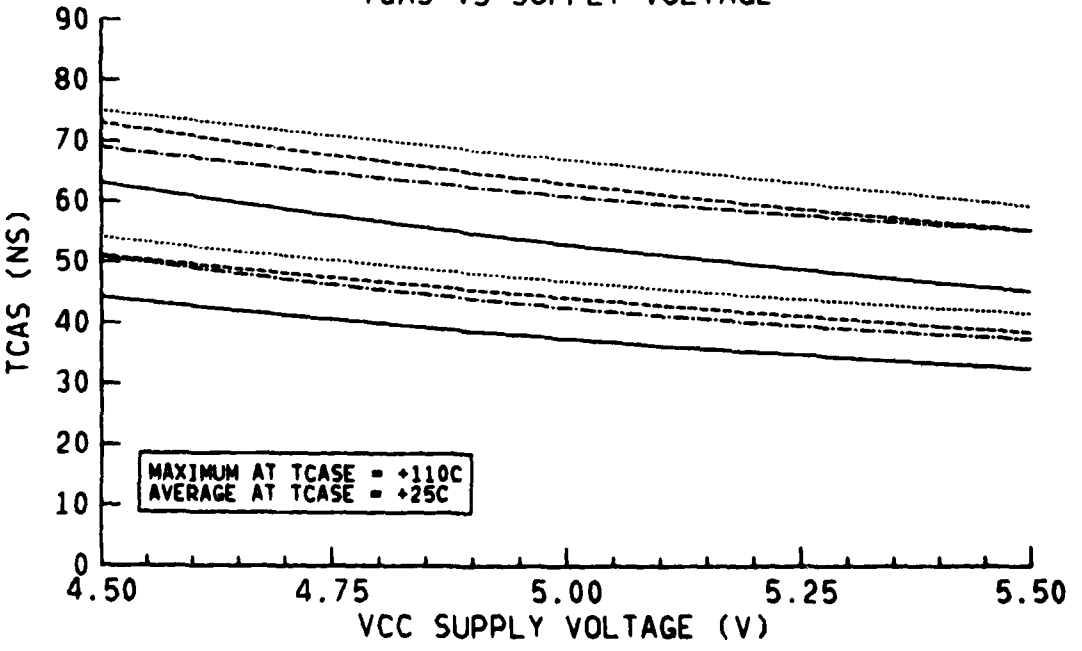
CAS PULSE WIDTH

PROPOSED LIMIT
90NS MIN

TCAS VS TEMPERATURE



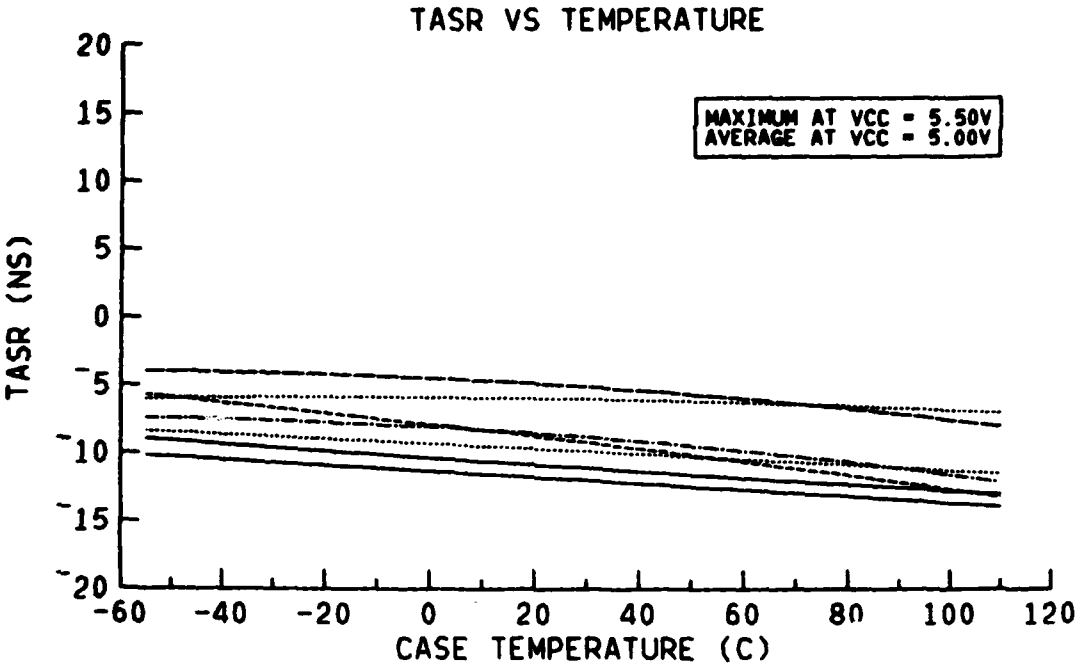
TCAS VS SUPPLY VOLTAGE

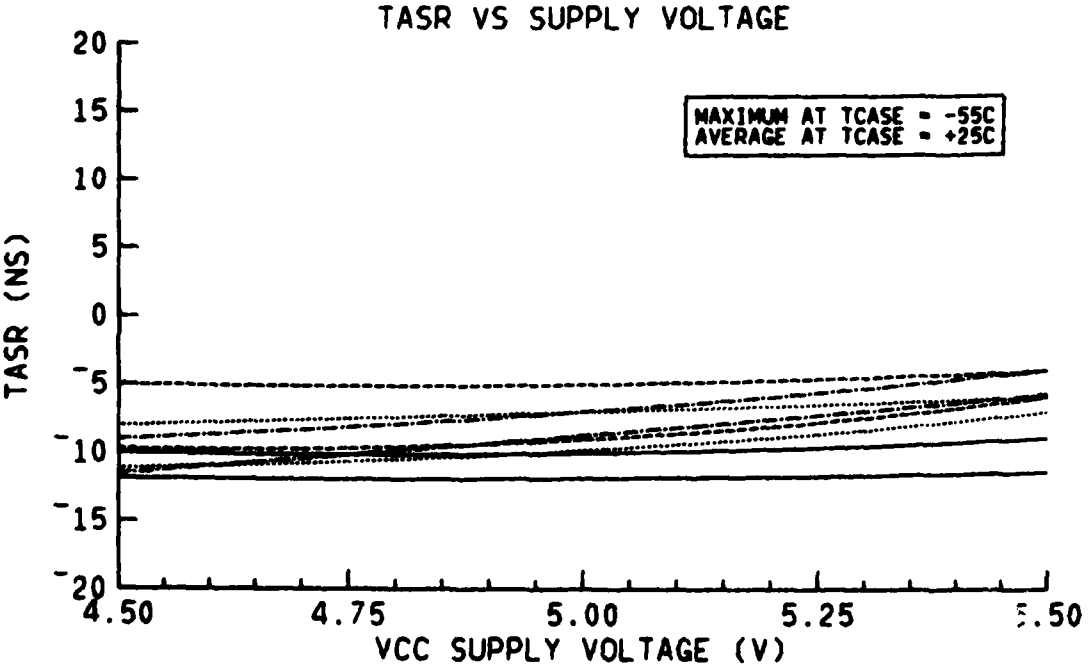


VENDOR A
VENDOR B
VENDOR C
VENDOR D

ROW ADDRESS SET-UP TIME

PROPOSED LIMIT
0NS MIN



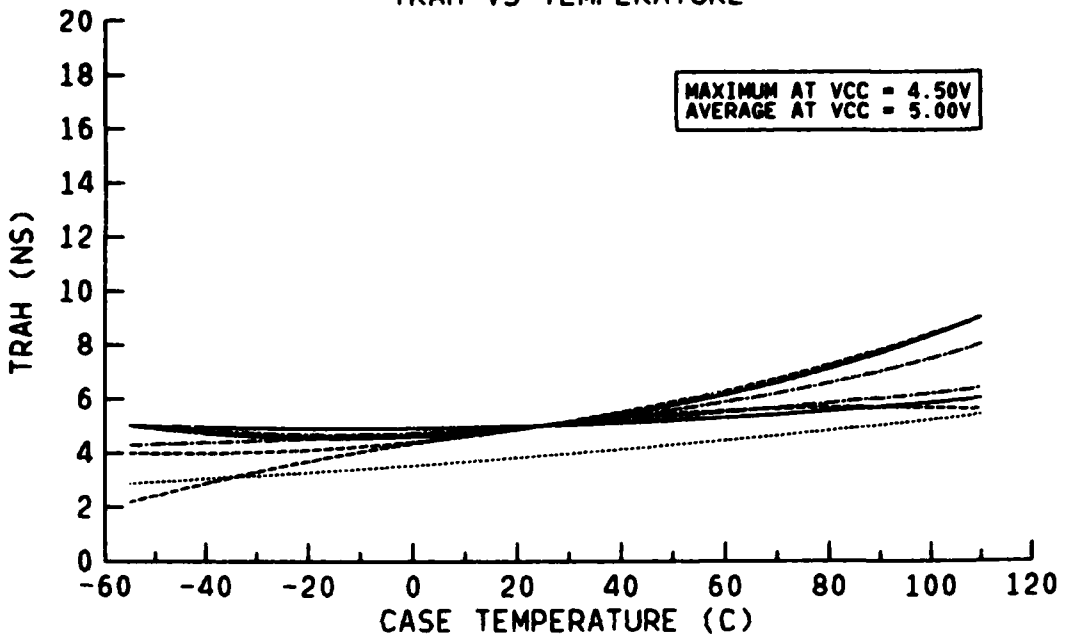


VENDOR A
VENDOR B
VENDOR C
VENDOR D

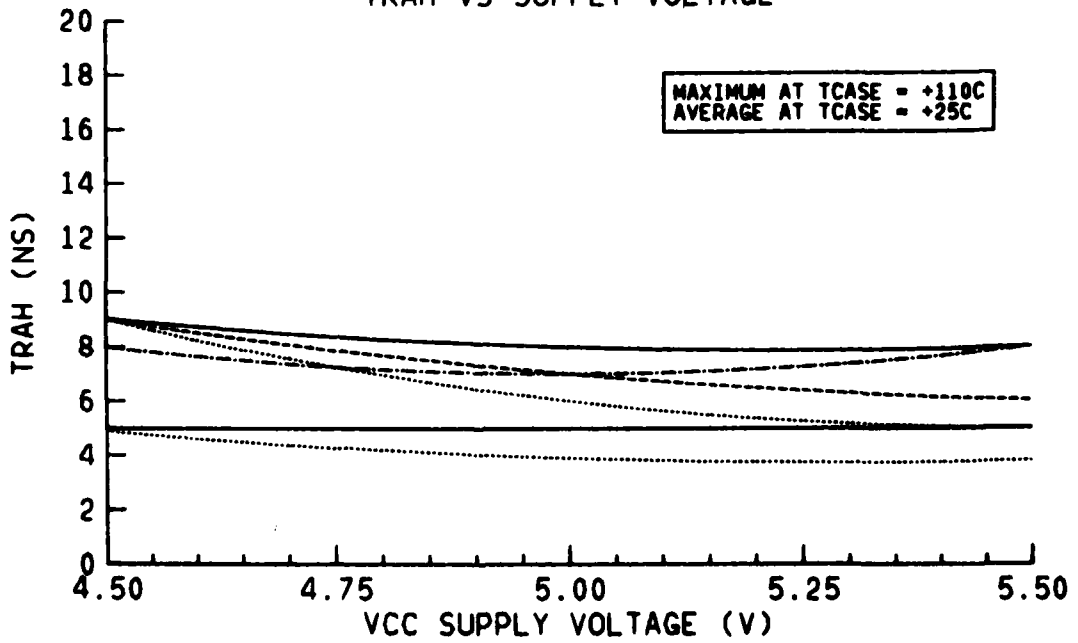
ROW ADDRESS HOLD TIME

PROPOSED LIMIT
20NS MIN

TRAH VS TEMPERATURE



TRAH VS SUPPLY VOLTAGE

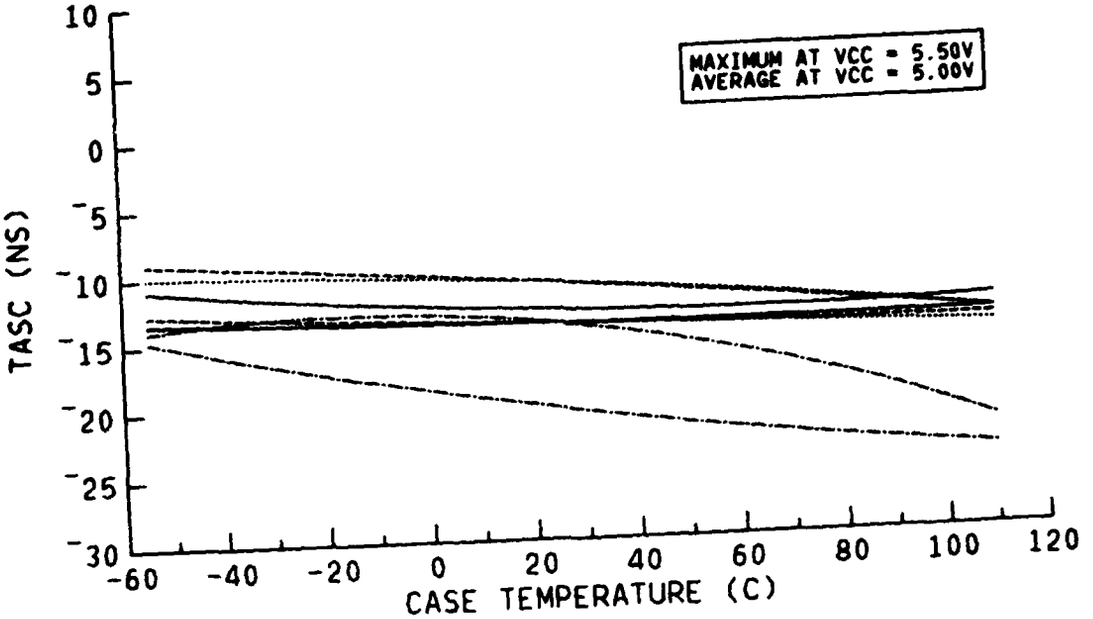


VENDOR A
VENDOR B
VENDOR C
VENDOR D

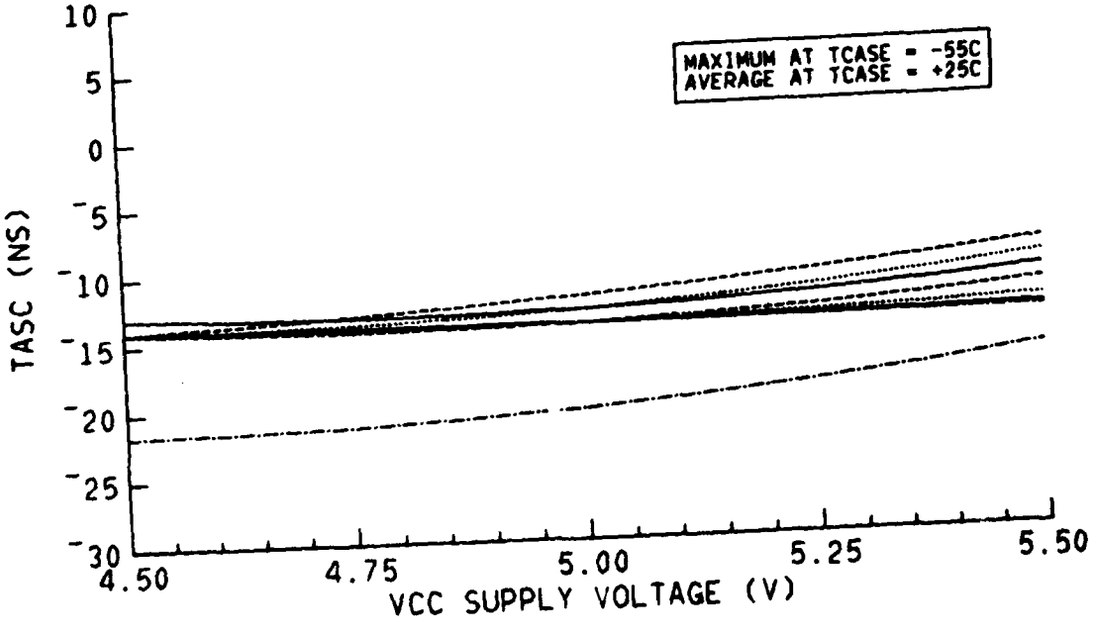
COLUMN ADDRESS SET-UP TIME

PROPOSED LIMIT
-5NS MIN

TASC VS TEMPERATURE



TASC VS SUPPLY VOLTAGE

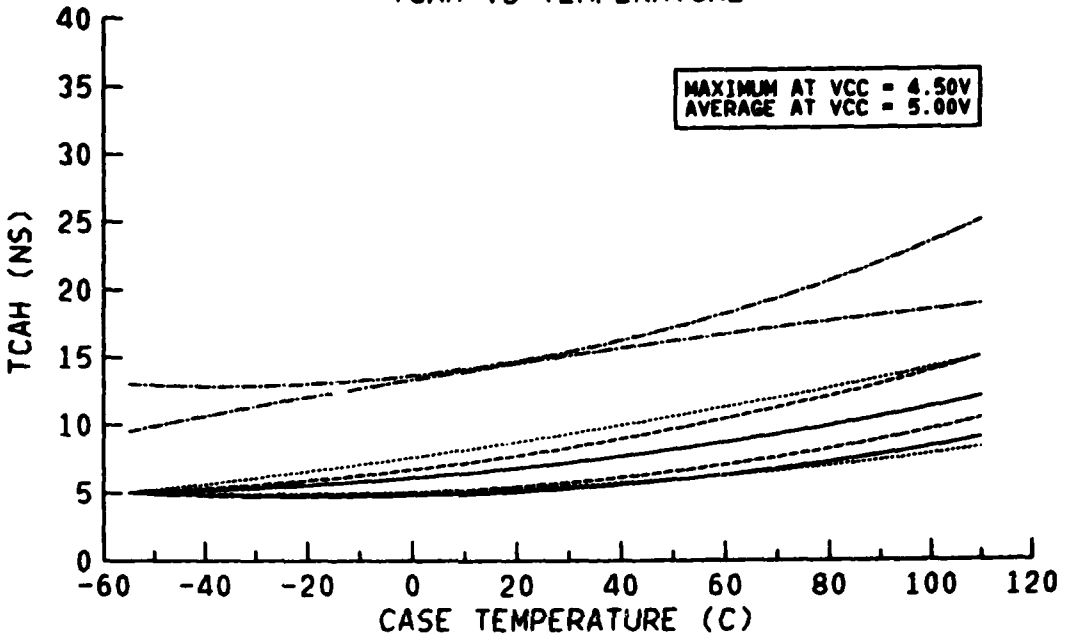


VENDOR A
VENDOR B
VENDOR C
VENDOR D

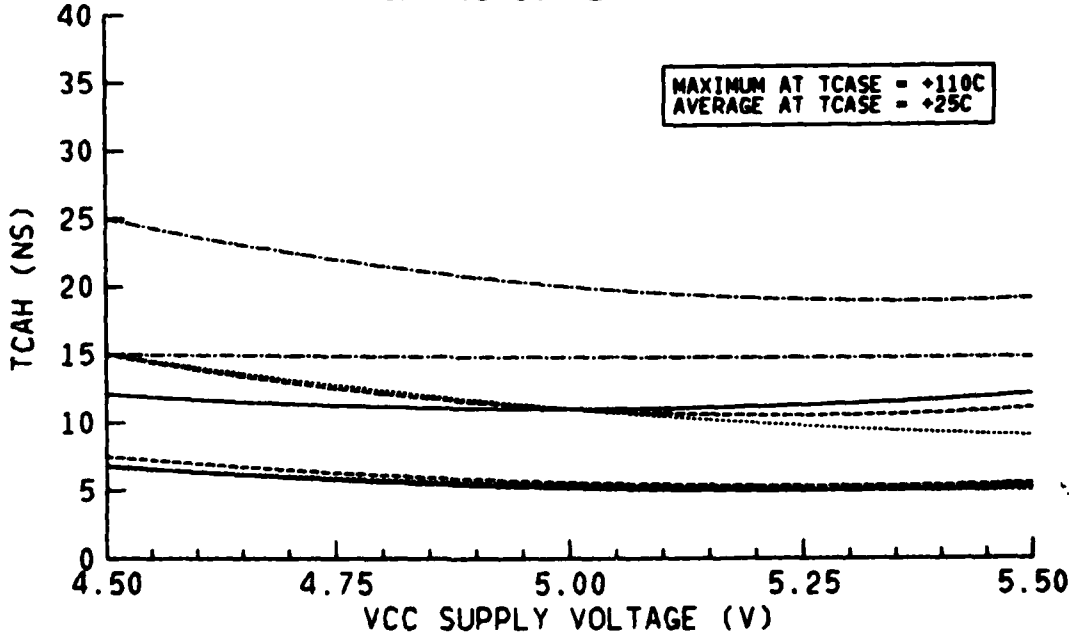
COLUMN ADDRESS HOLD TIME

PROPOSED LIMIT
30NS MIN

TCAH VS TEMPERATURE



TCAH VS SUPPLY VOLTAGE

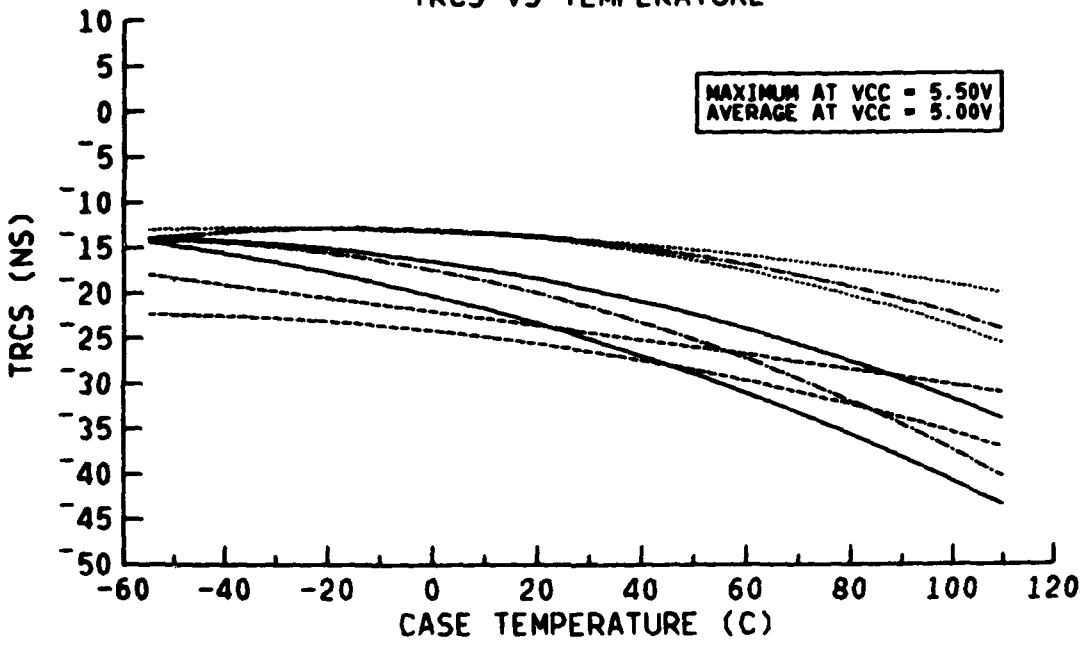


VENDOR A
VENDOR B
VENDOR C
VENDOR D

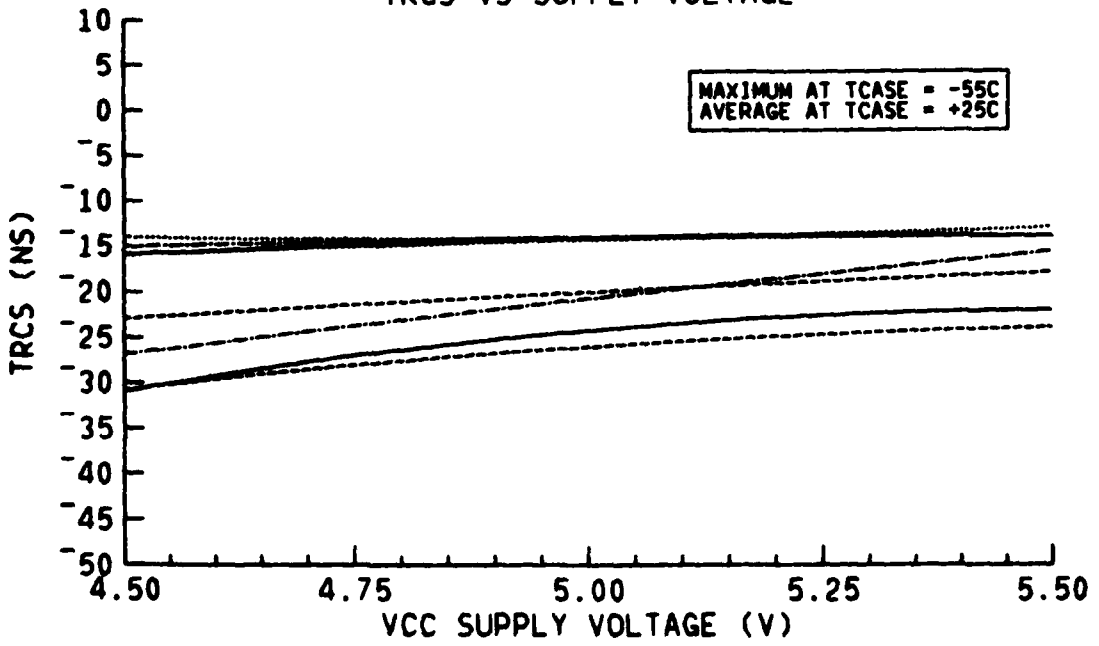
READ COMMAND SET-UP TIME

PROPOSED LIMIT
0NS MIN

TRCS VS TEMPERATURE



TRCS VS SUPPLY VOLTAGE

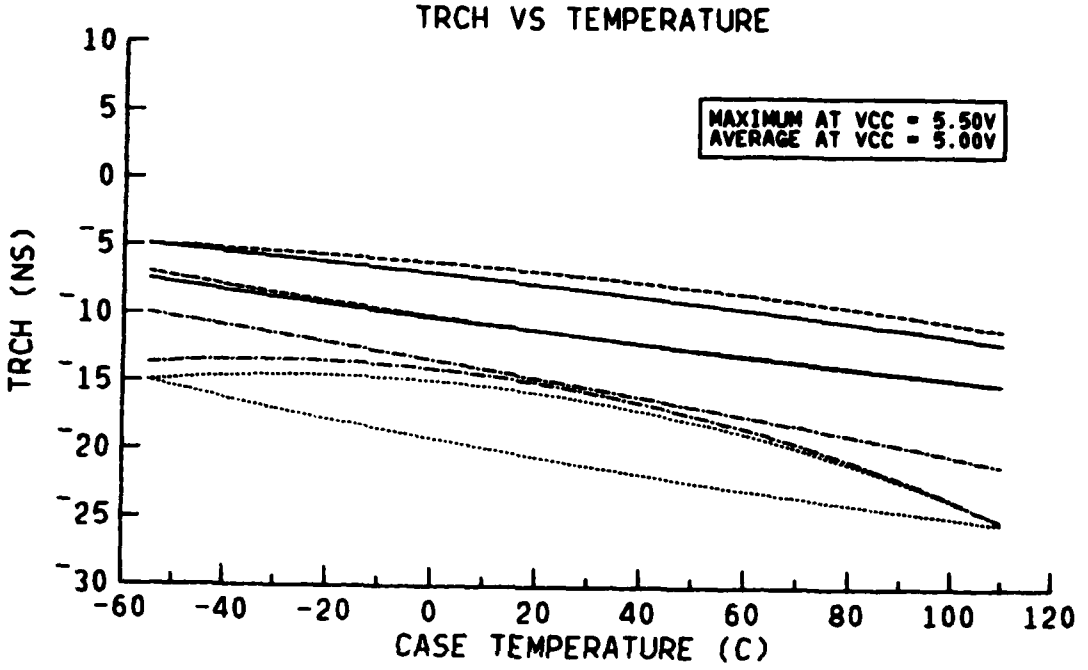


VENDOR A
VENDOR B
VENDOR C
VENDOR D

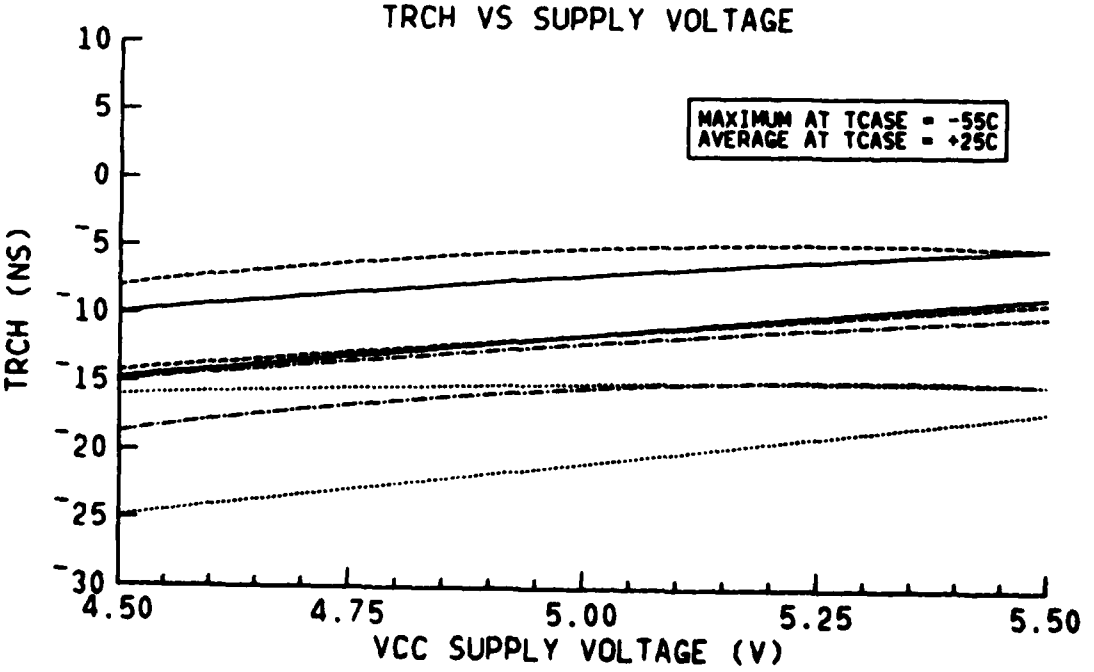
READ COMMAND HOLD TIME

PROPOSED LIMIT
0NS MIN

TRCH VS TEMPERATURE



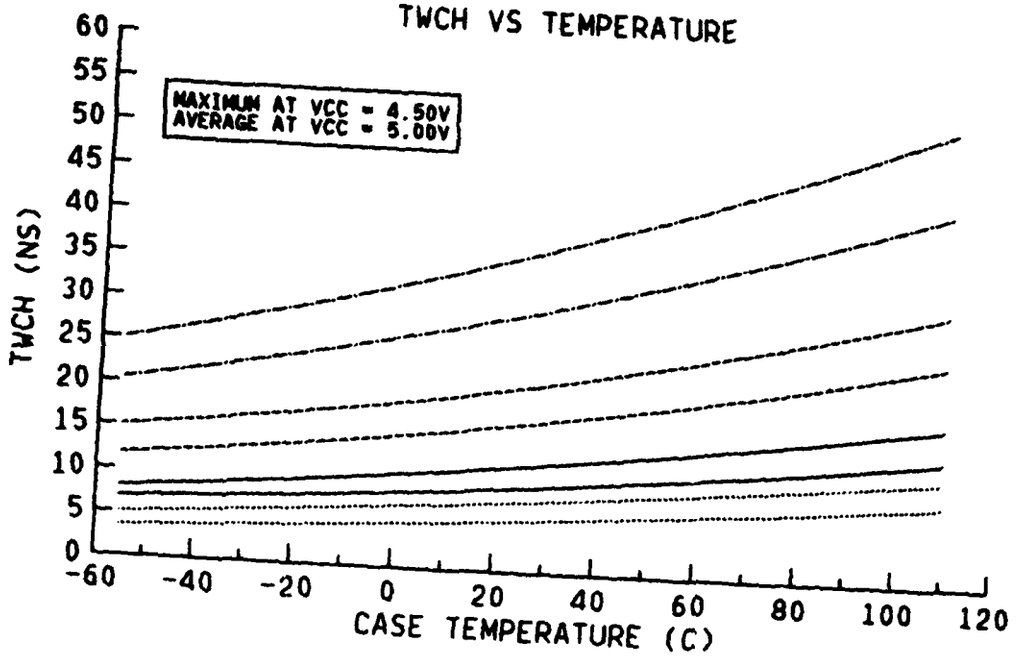
TRCH VS SUPPLY VOLTAGE

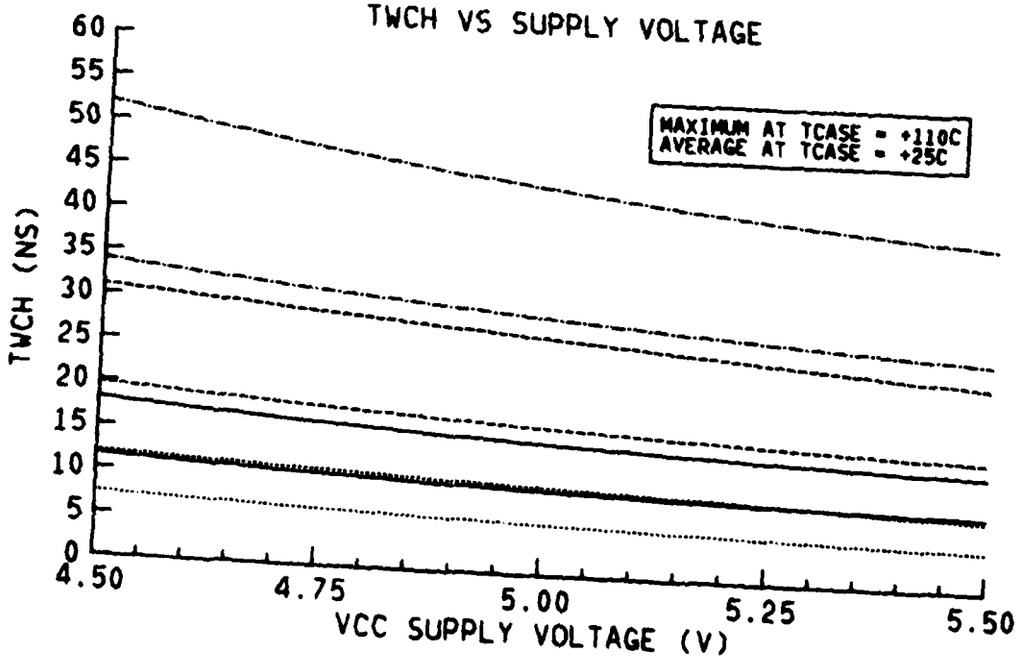


VENDOR A
VENDOR B
VENDOR C
VENDOR D

WRITE COMMAND HOLD TIME

PROPOSED LIMIT
45NS MIN



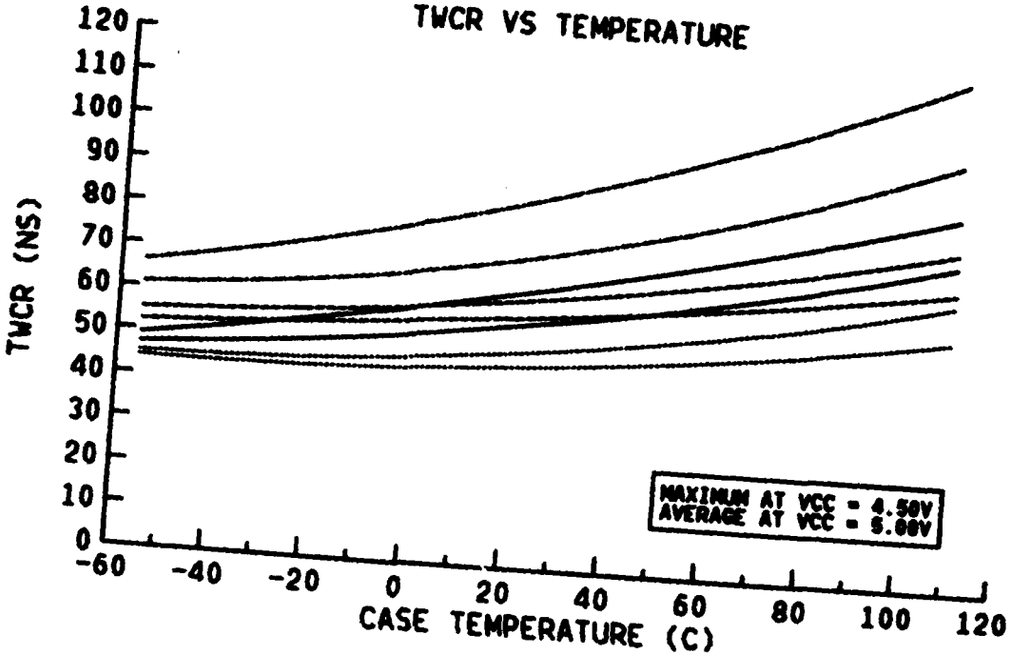


VENDOR A
VENDOR B
VENDOR C
VENDOR D

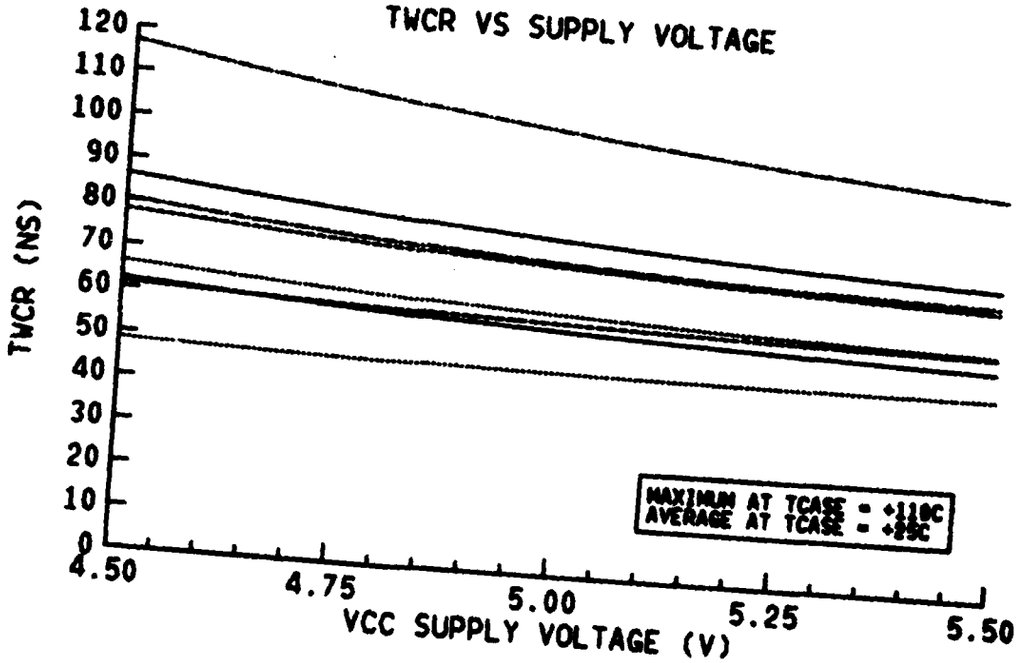
WRITE COMMAND HOLD TIME REFERENCED TO RAS

PROPOSED LIMIT
120NS MIN

TWCR VS TEMPERATURE



TWCR VS SUPPLY VOLTAGE

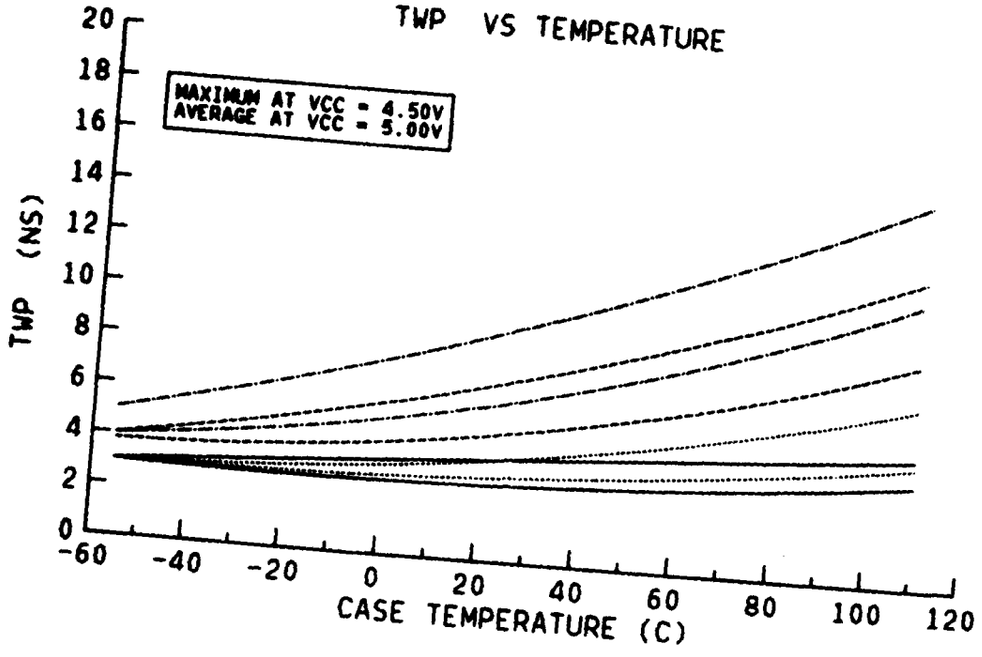


VENDOR A
VENDOR B
VENDOR C
VENDOR D

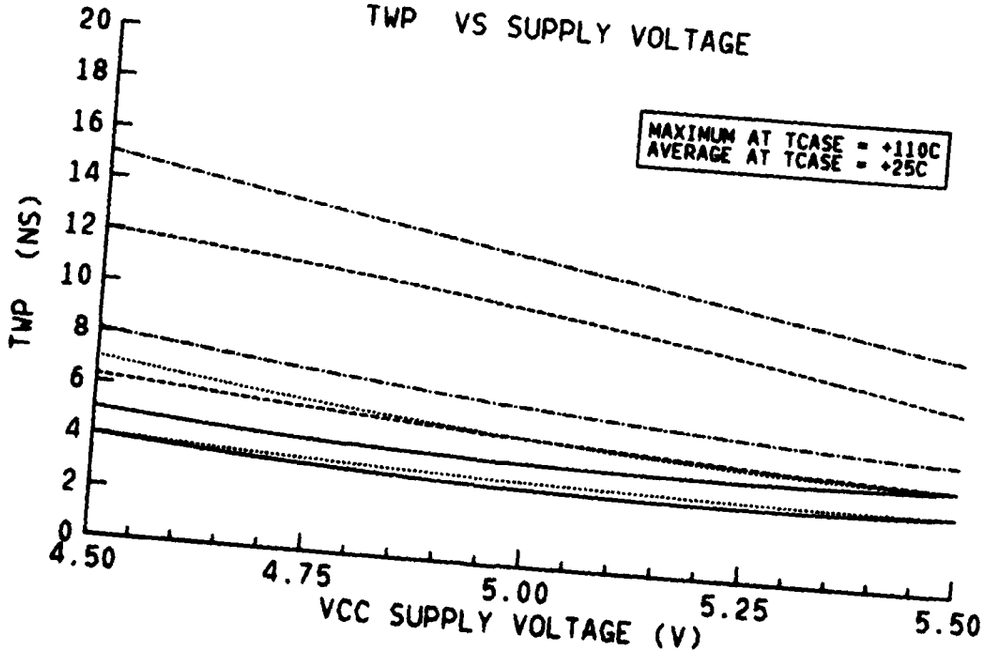
WRITE COMMAND PULSE WIDTH

PROPOSED LIMIT
45NS MIN

TWP VS TEMPERATURE



TWP VS SUPPLY VOLTAGE

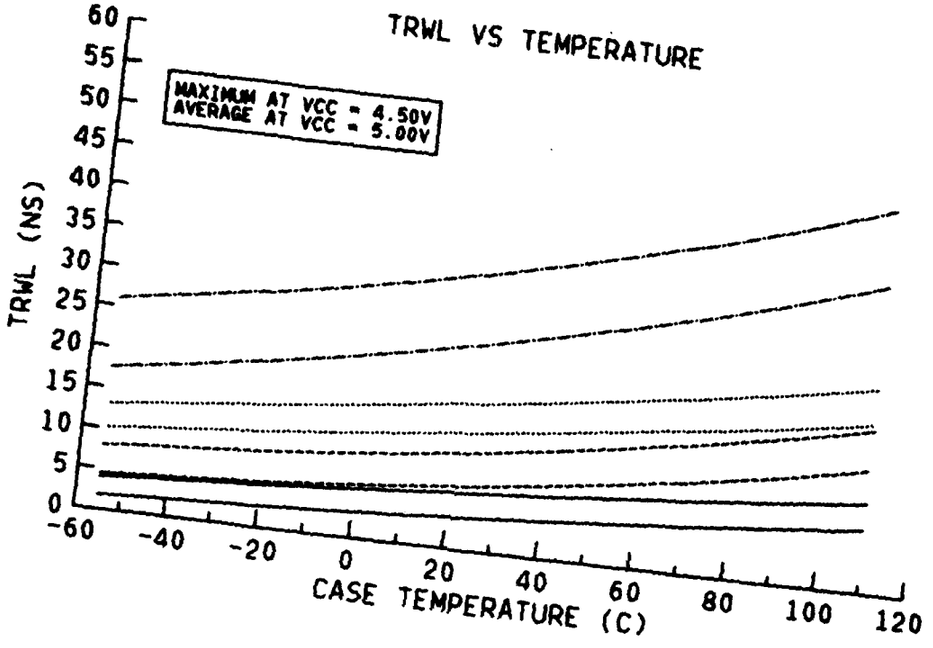


VENDOR A
VENDOR B
VENDOR C
VENDOR D

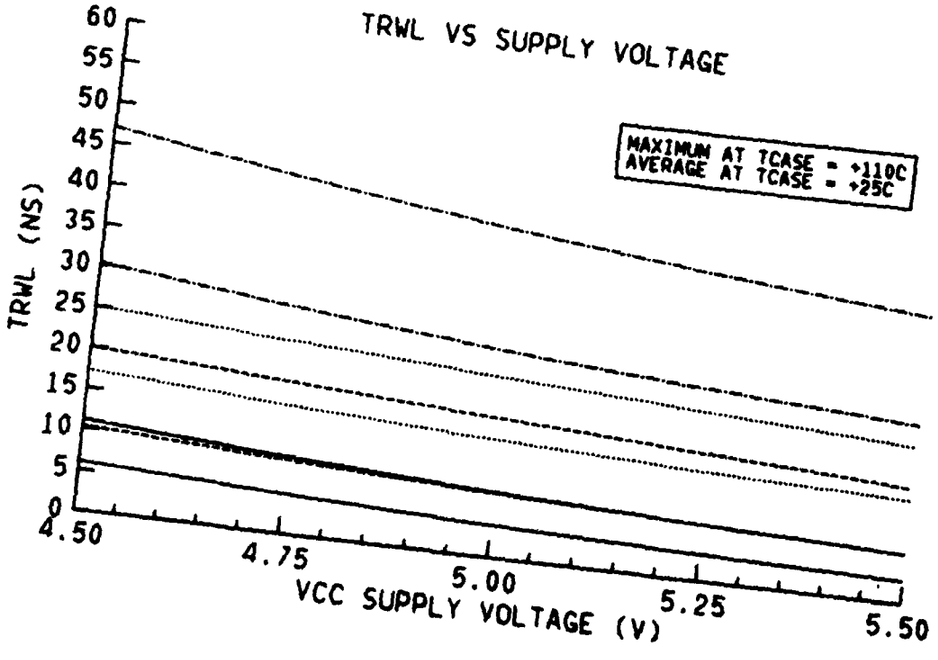
WRITE COMMAND TO RAS LEAD TIME

PROPOSED LIMIT
45NS MIN

TRWL VS TEMPERATURE



TRWL VS SUPPLY VOLTAGE

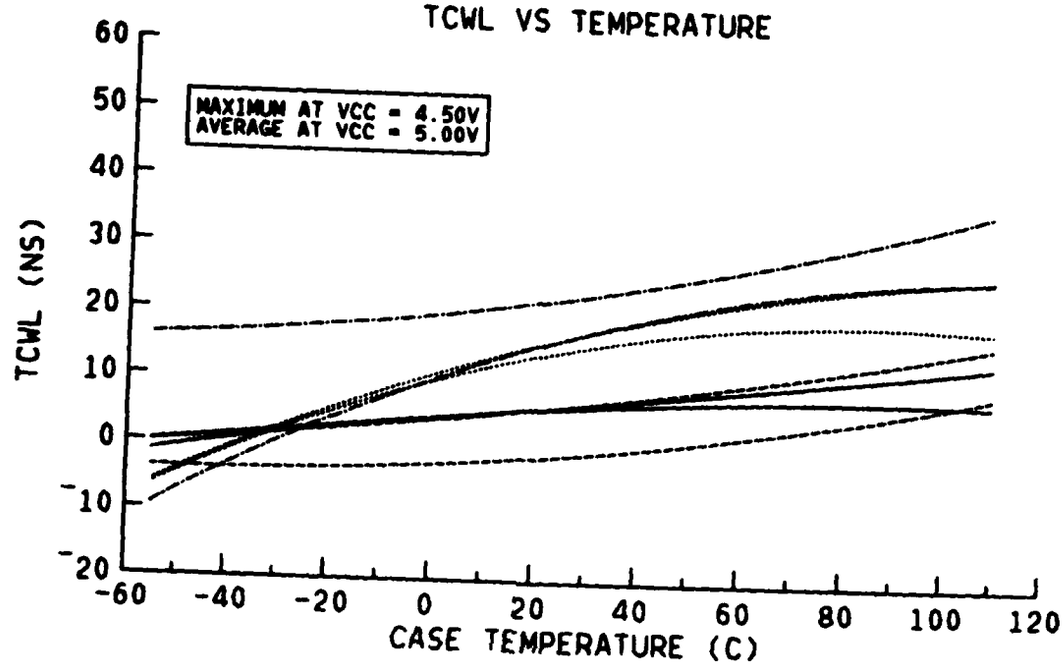


VENDOR A
VENDOR B
VENDOR C
VENDOR D

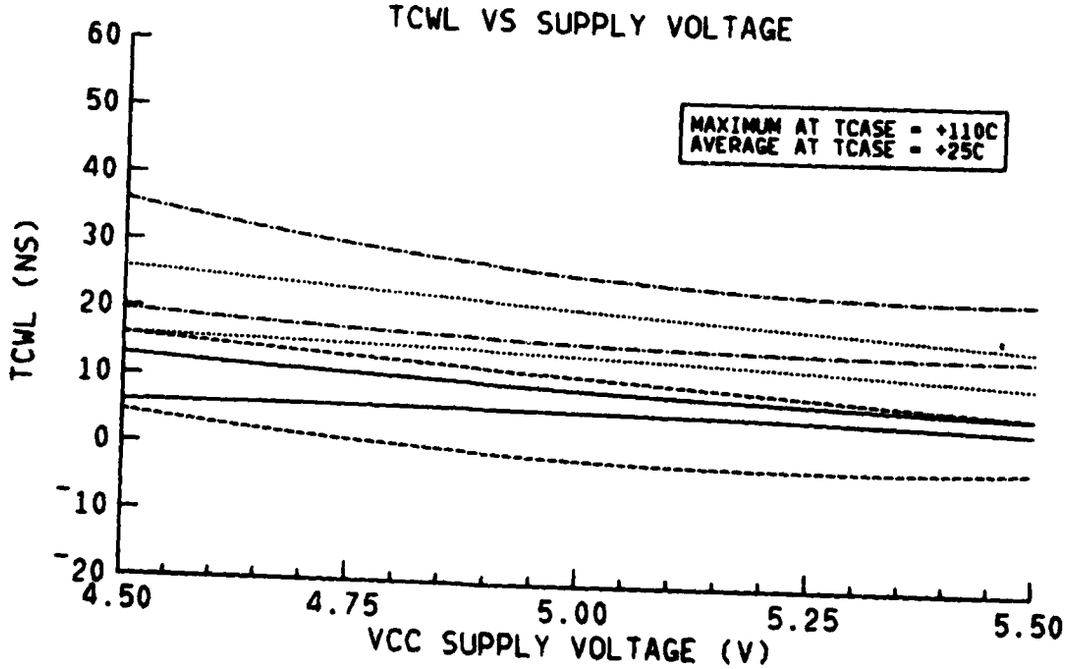
WRITE COMMAND TO CAS LEAD TIME

PROPOSED LIMIT
45NS MIN

TCWL VS TEMPERATURE



TCWL VS SUPPLY VOLTAGE

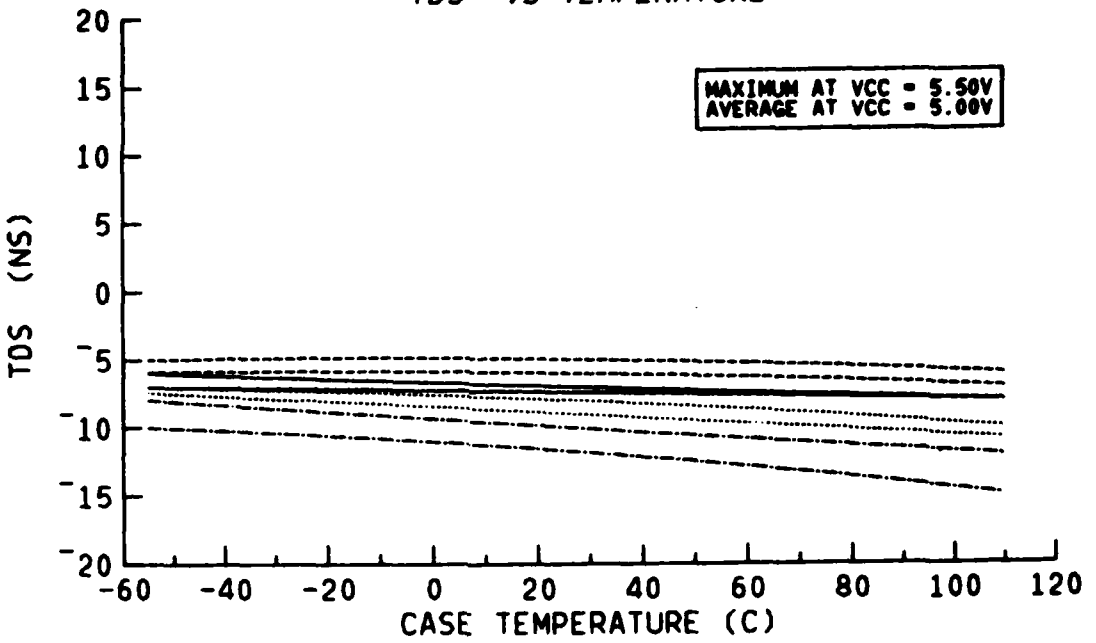


VENDOR A
VENDOR B
VENDOR C
VENDOR D

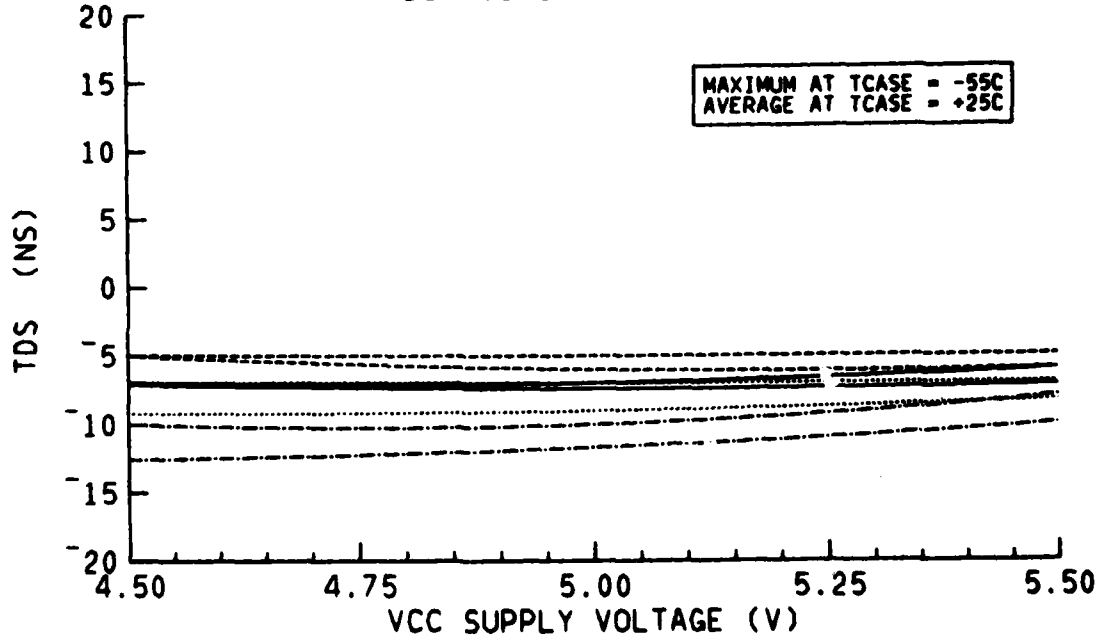
DATA IN SET-UP TIME

PROPOSED LIMIT
0NS MIN

TDS VS TEMPERATURE



TDS VS SUPPLY VOLTAGE

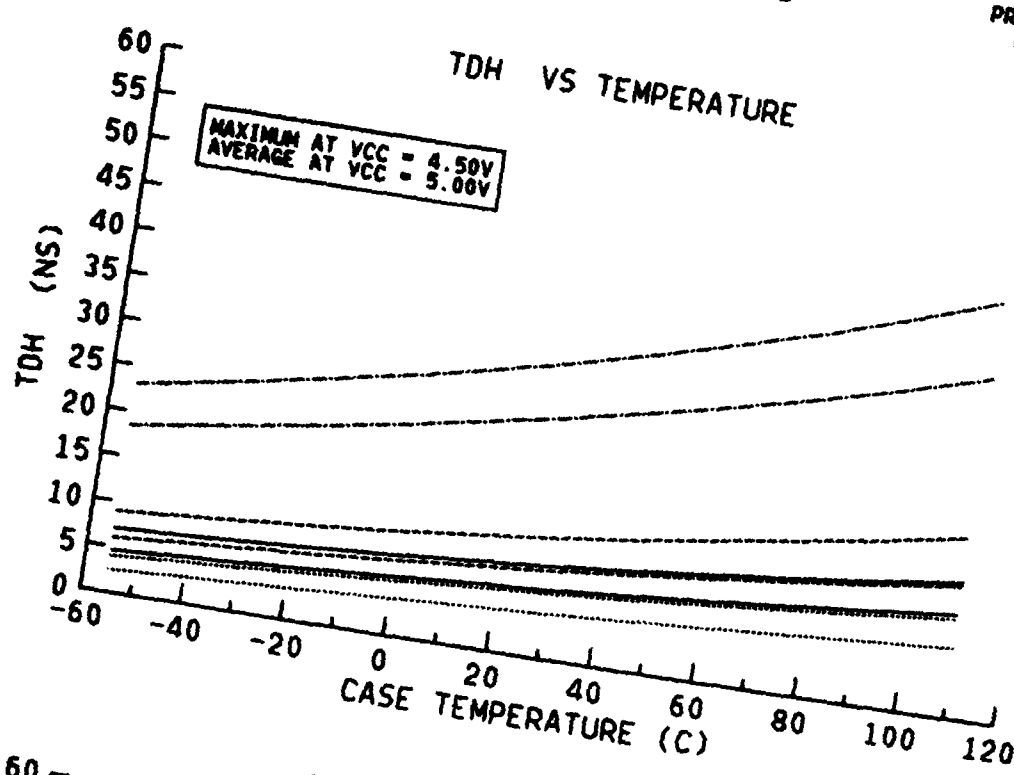


VENDOR A
VENDOR B
VENDOR C
VENDOR D

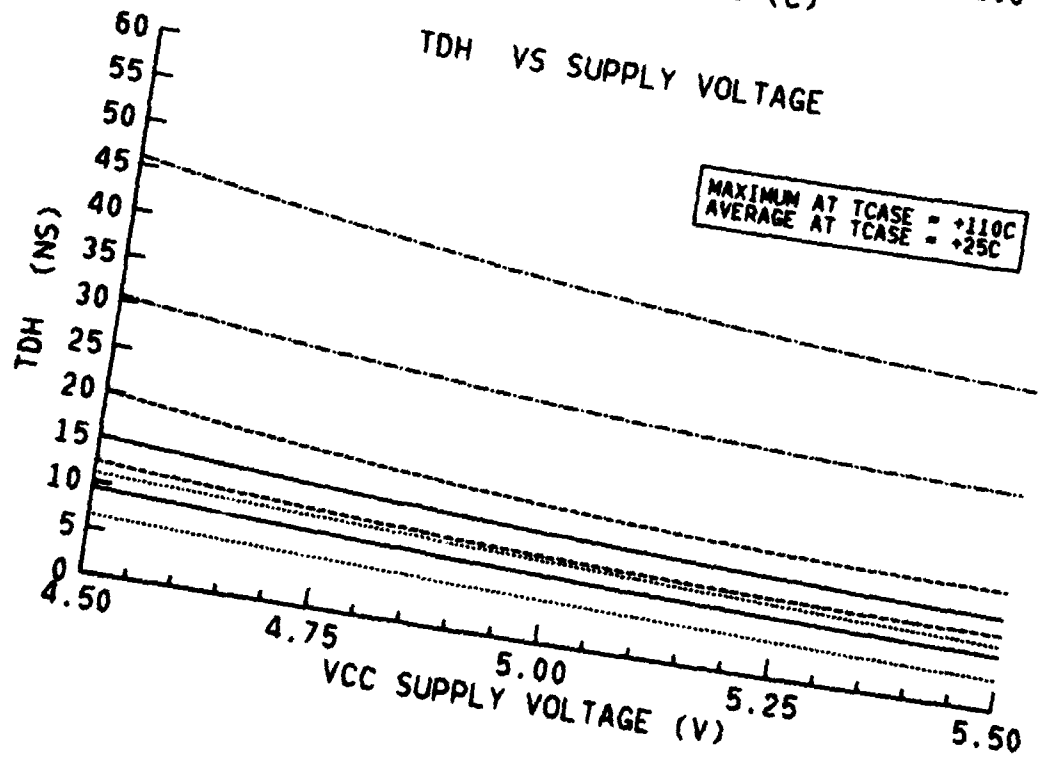
DATA IN HOLD TIME

PROPOSED LIMIT
45NS MIN

TDH VS TEMPERATURE



TDH VS SUPPLY VOLTAGE

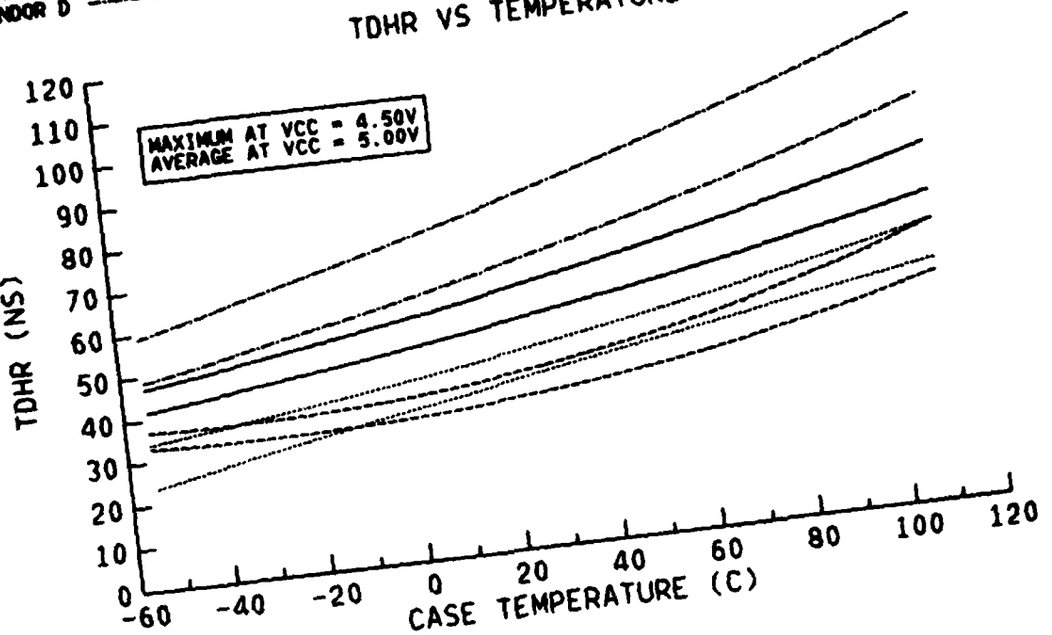


DATA IN HOLD TIME

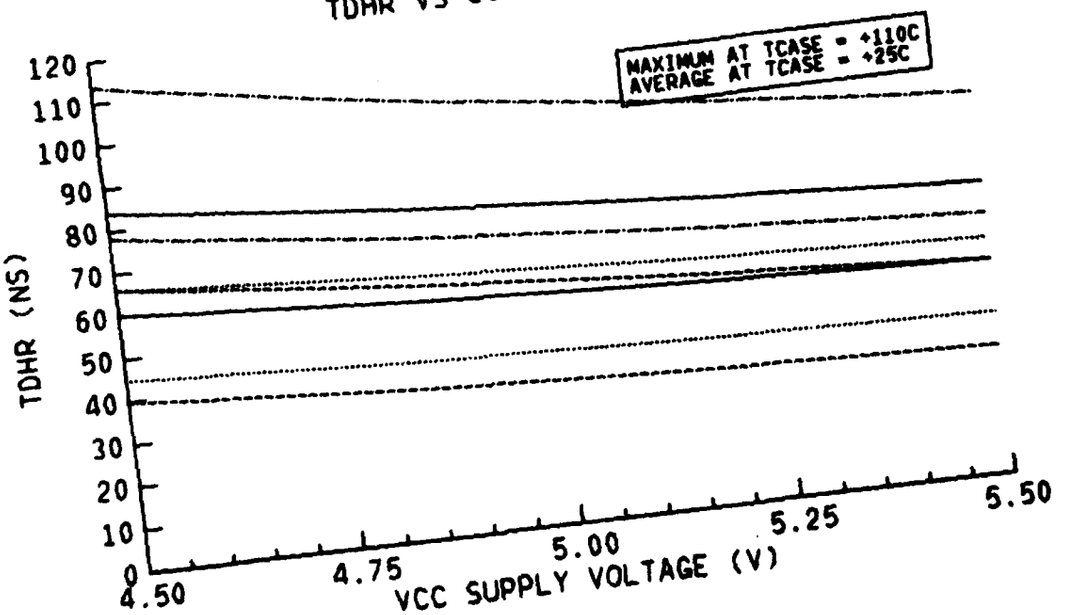
PROPOSED LIMIT
120NS MIN

VENDOR A
VENDOR B
VENDOR C
VENDOR D

TDHR VS TEMPERATURE



TDHR VS SUPPLY VOLTAGE

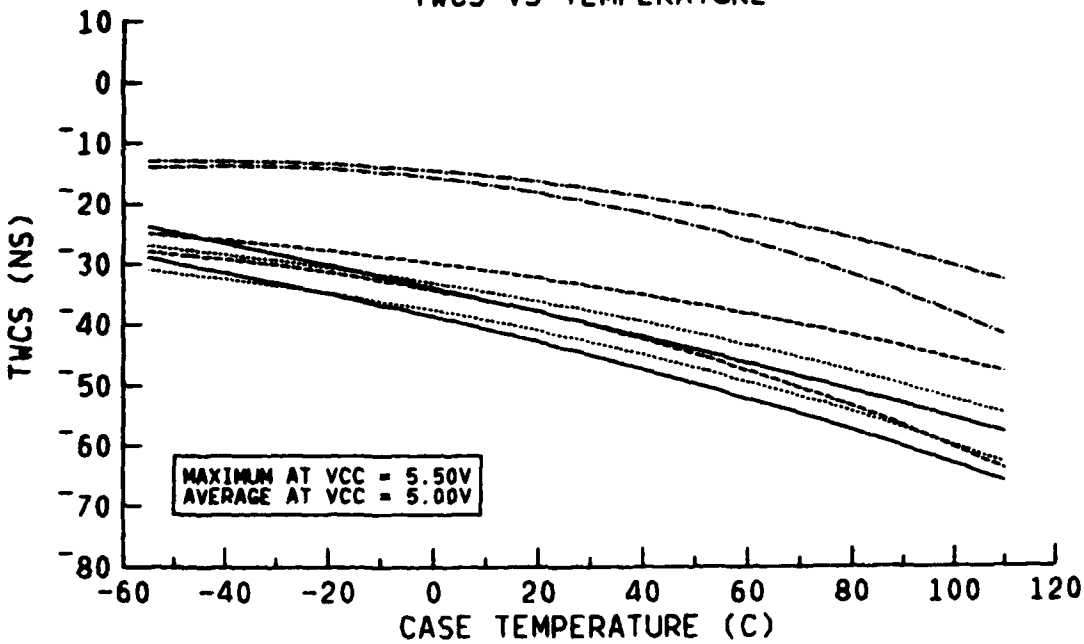


VENDOR A
VENDOR B
VENDOR C
VENDOR D

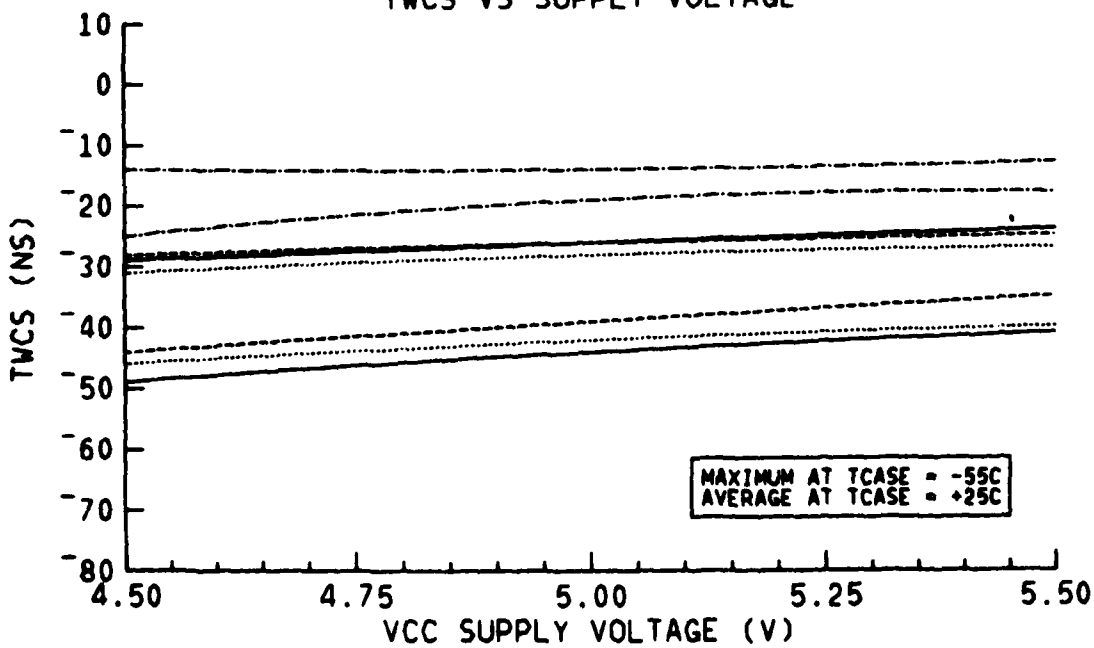
WRITE COMMAND SET-UP TIME

PROPOSED LIMIT
0NS MIN

TWCS VS TEMPERATURE



TWCS VS SUPPLY VOLTAGE

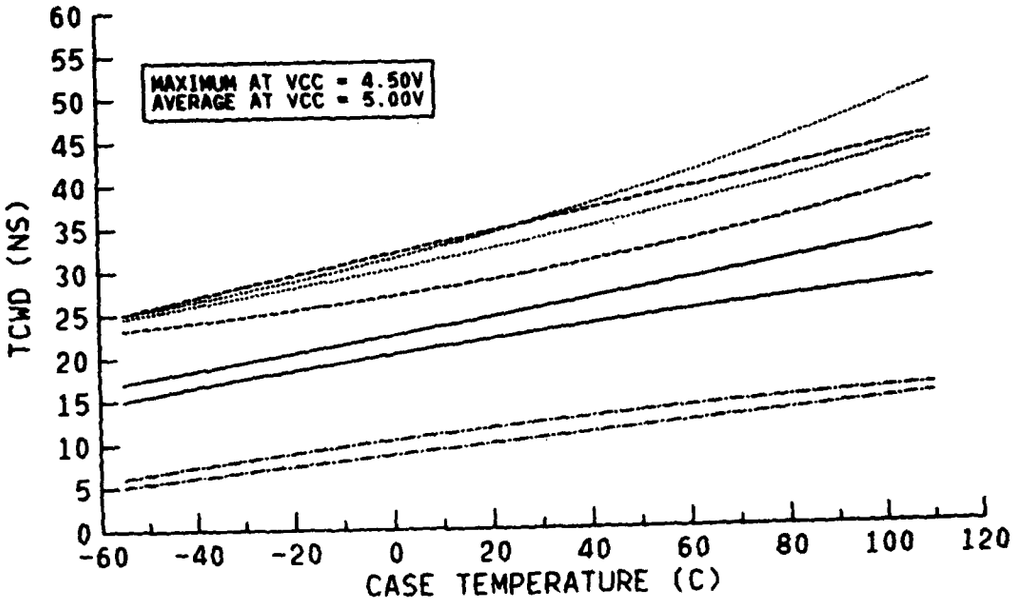


VENDOR A
VENDOR B
VENDOR C
VENDOR D

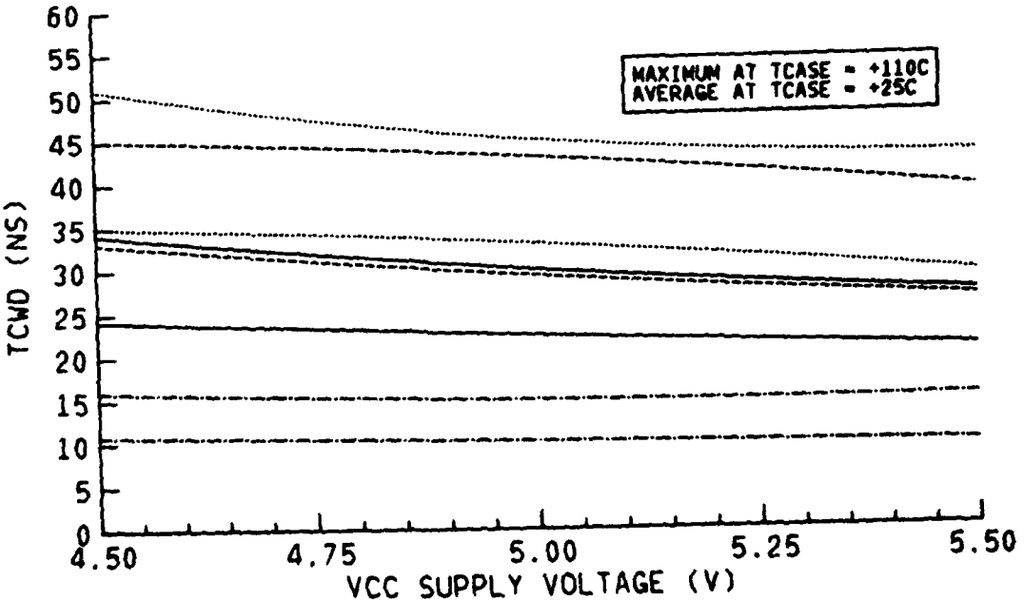
CAS TO WRITE DELAY

PROPOSED LIMIT
50NS MIN

TCWD VS TEMPERATURE



TCWD VS SUPPLY VOLTAGE

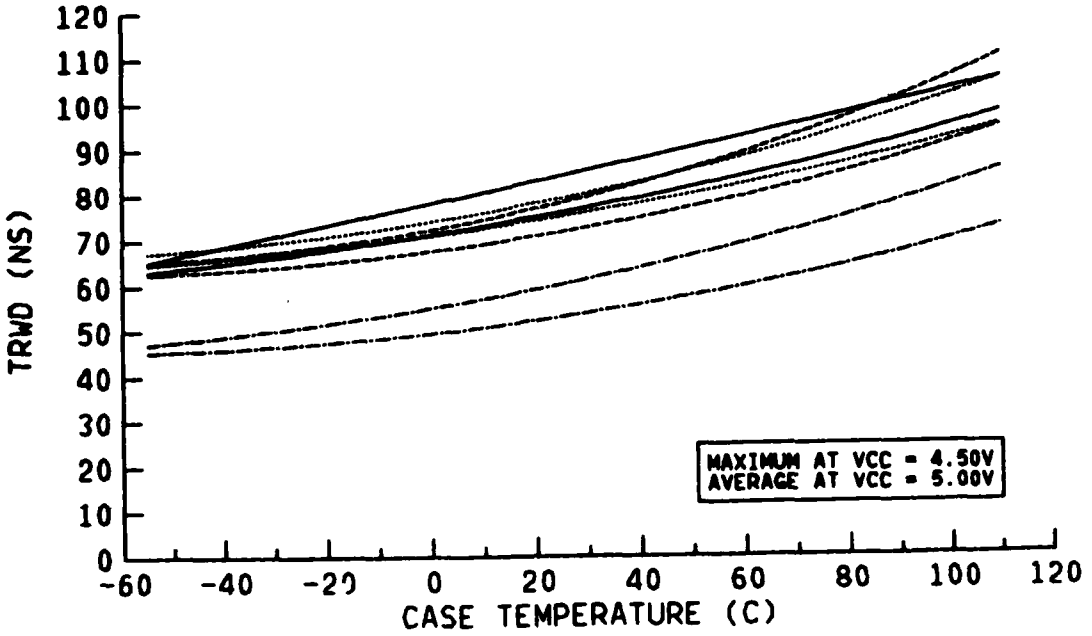


VENDOR A
VENDOR B
VENDOR C
VENDOR D

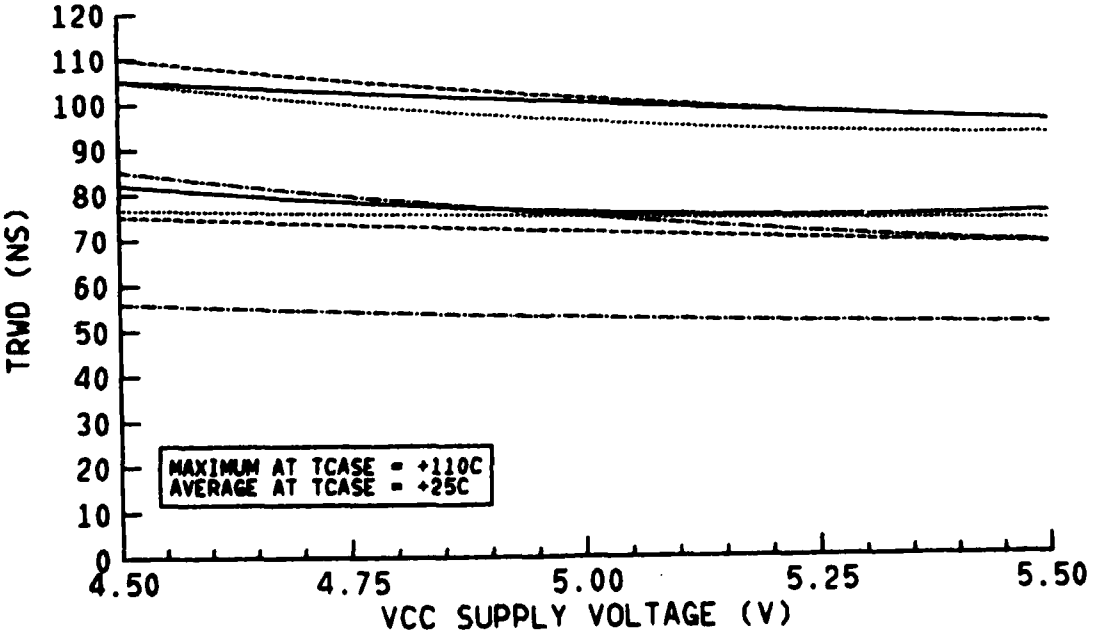
RAS TO WRITE DELAY

PROPOSED LIMIT
110NS MIN

TRWD VS TEMPERATURE



TRWD VS SUPPLY VOLTAGE

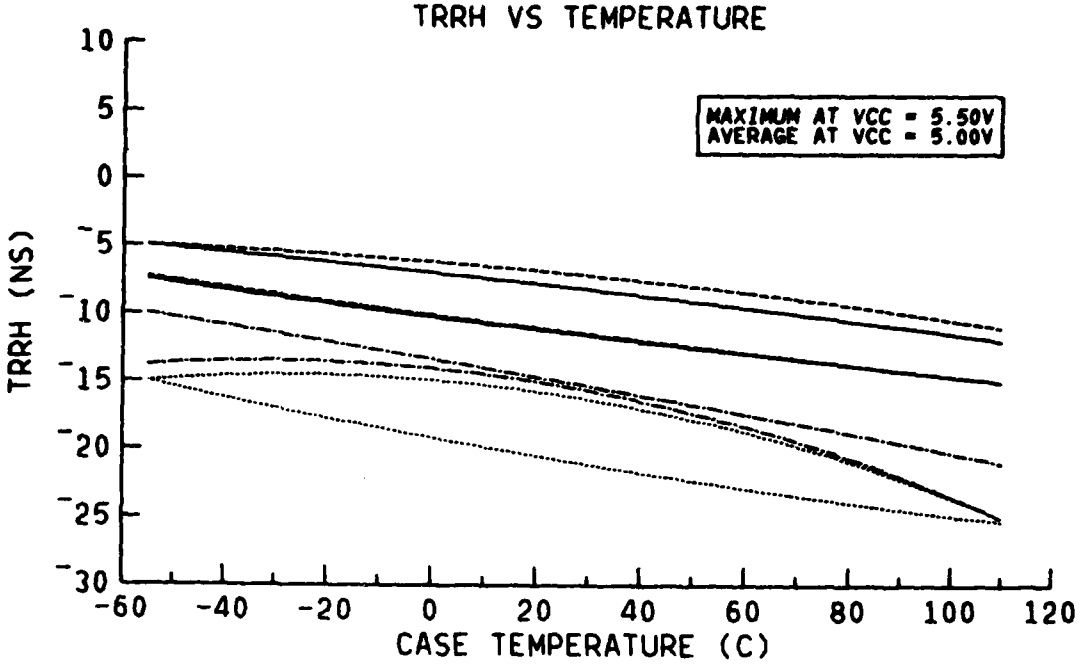


VENDOR A
VENDOR B
VENDOR C
VENDOR D

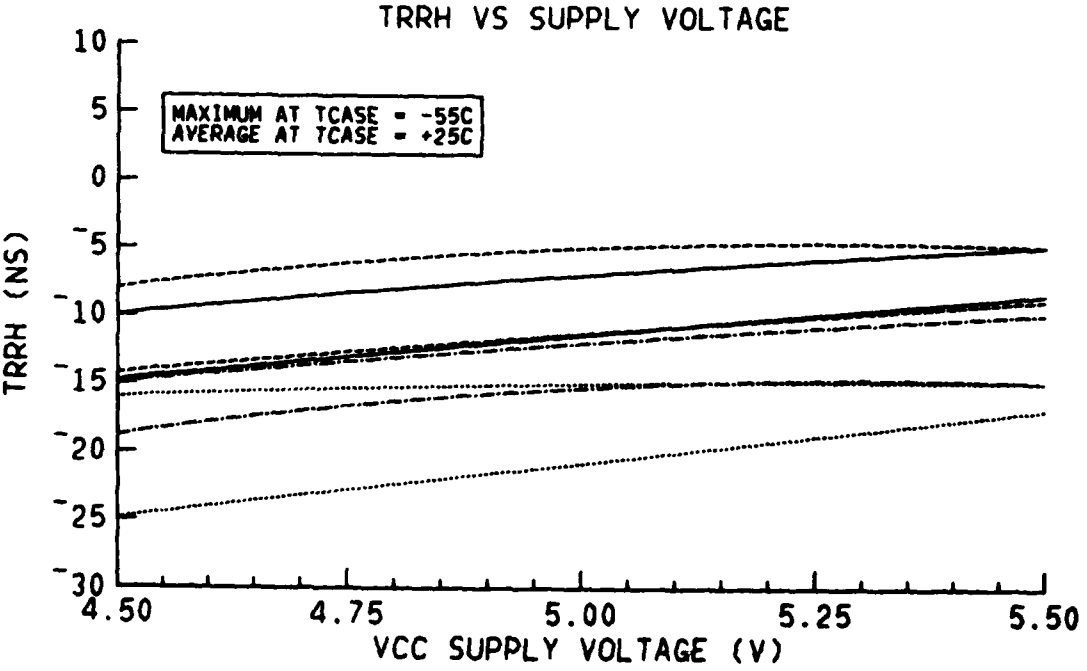
READ COMMAND HOLD TIME REFERENCED TO RAS

PROPOSED LIMIT
25NS MIN

TRRH VS TEMPERATURE



TRRH VS SUPPLY VOLTAGE



APPENDIX II

SUPPLY CURRENT GRAPHS

NOTE: Supply current measurements shown appear in the following order:

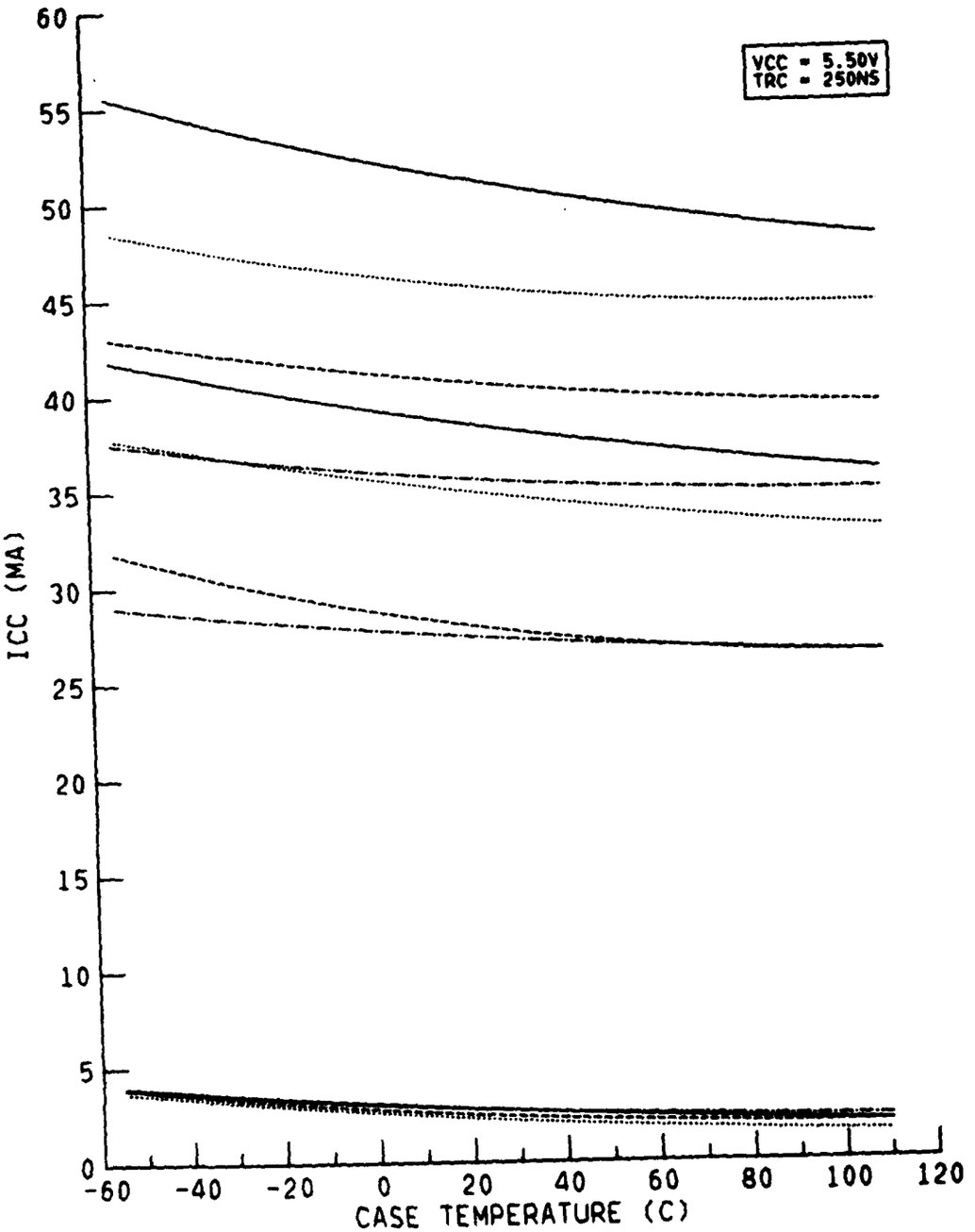
Upper Curve - $\overline{RAS}/\overline{CAS}$ cycling (ICC1)
Middle Curve - $\overline{RAS}$-only refresh (ICC3)
Lower Curve - Standby (ICC2)

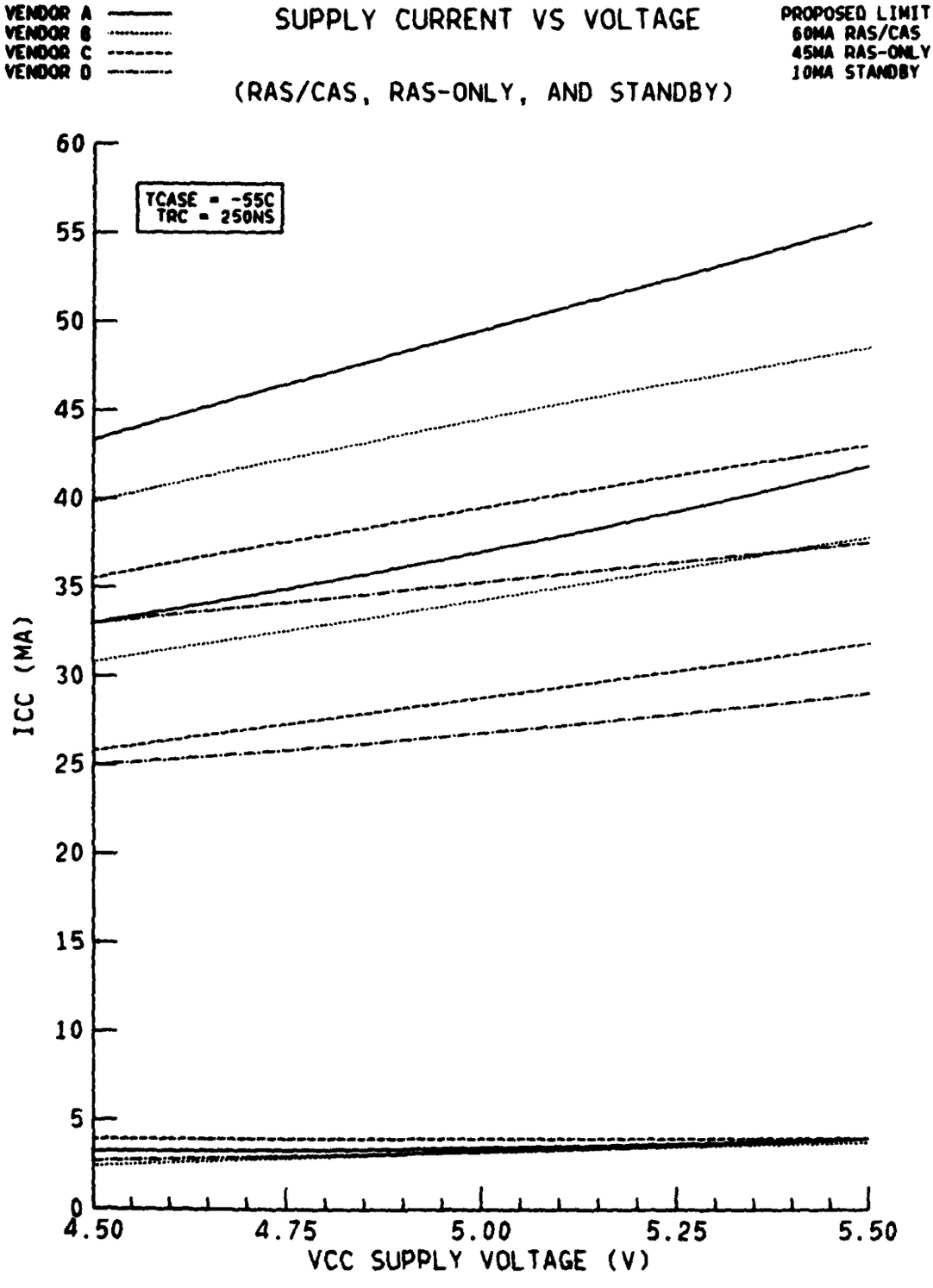
VENDOR A
VENDOR B
VENDOR C
VENDOR D

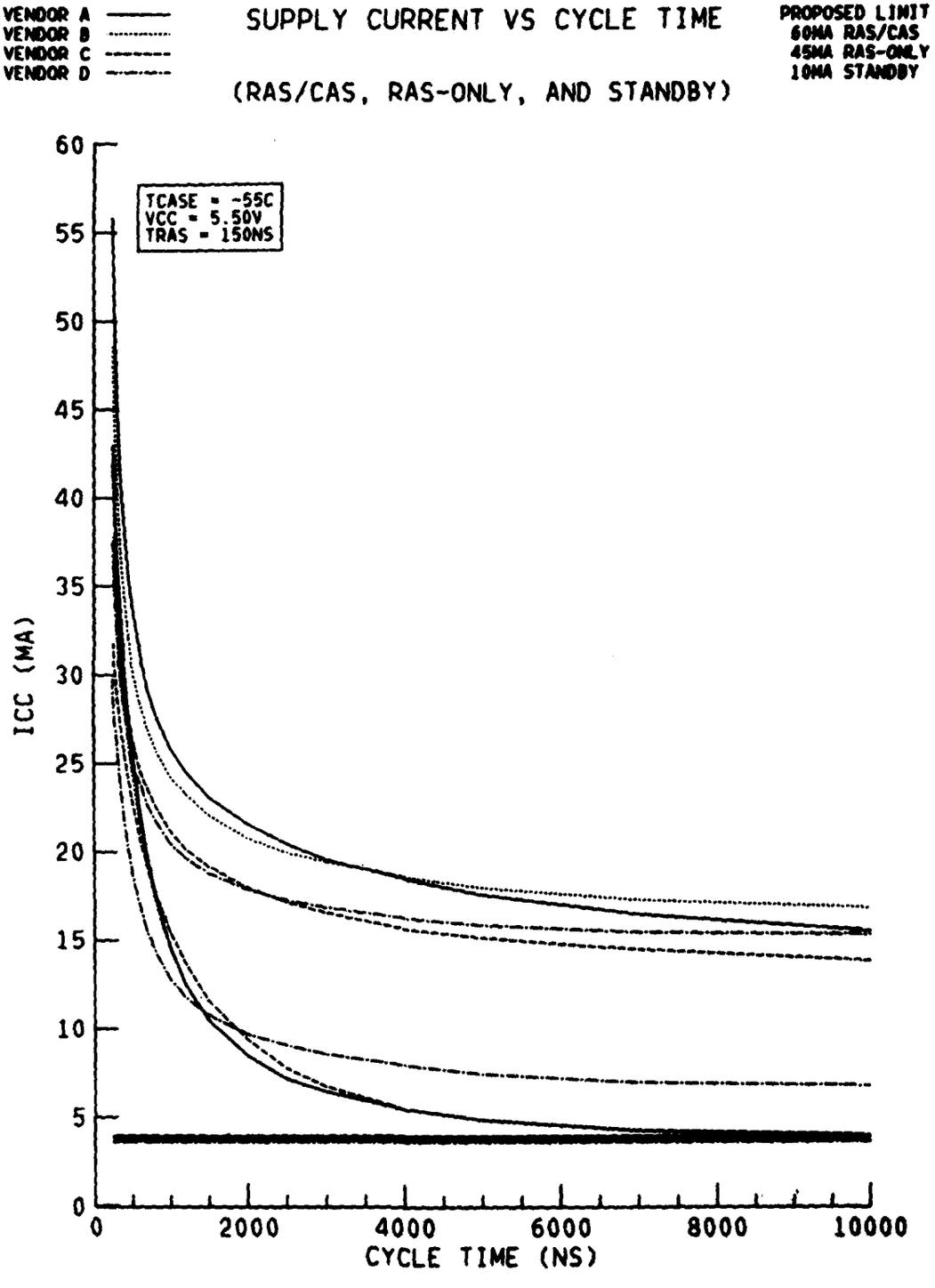
SUPPLY CURRENT VS TEMPERATURE

(RAS/CAS, RAS-ONLY, AND STANDBY)

PROPOSED LIMIT
60MA RAS/CAS
45MA RAS-ONLY
10MA STANDBY




VENDOR A
VENDOR B
VENDOR C
VENDOR D
SUPPLY CURRENT VS VOLTAGE
(RAS/CAS, RAS-ONLY, AND STANDBY)
PROPOSED LIMIT
60MA RAS/CAS
45MA RAS-ONLY
10MA STANDBY
TCASE = -55C
TRC = 250NS
ICC (MA)
60
55
50
45
40
35
30
25
20
15
10
5
0
4.50
4.75
5.00
5.25
5.50
VCC SUPPLY VOLTAGE (V)

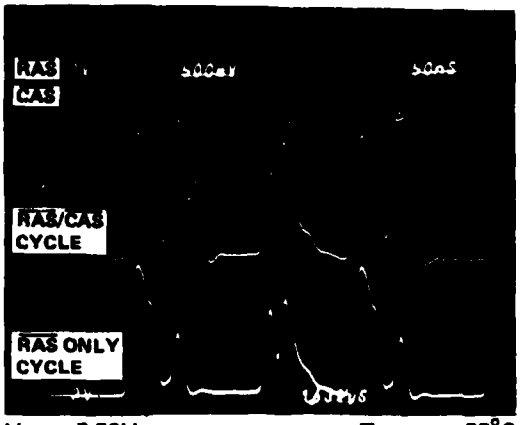

VENDOR A
VENDOR B
VENDOR C
VENDOR D
SUPPLY CURRENT VS CYCLE TIME
(RAS/CAS, RAS-ONLY, AND STANDBY)
PROPOSED LIMIT
60MA RAS/CAS
45MA RAS-ONLY
10MA STANDBY
TCASE = -55C
VCC = 5.50V
TRAS = 150NS
ICC (MA)
60
55
50
45
40
35
30
25
20
15
10
5
0
0
2000
4000
6000
8000
10000
CYCLE TIME (NS)

POWER SUPPLY TRANSIENT CURRENT

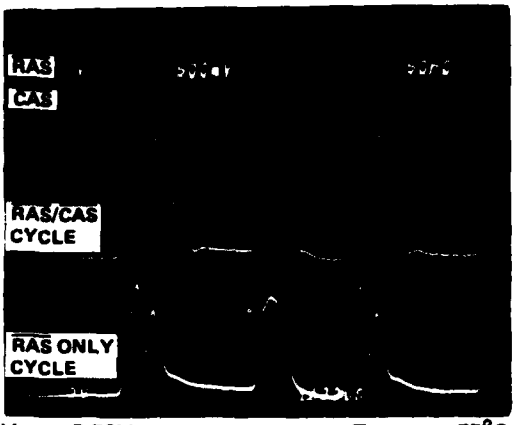
VENDOR A

50 MA/DIV. VERTICAL
50 NS/ DIV. HORIZONTAL

VENDOR B

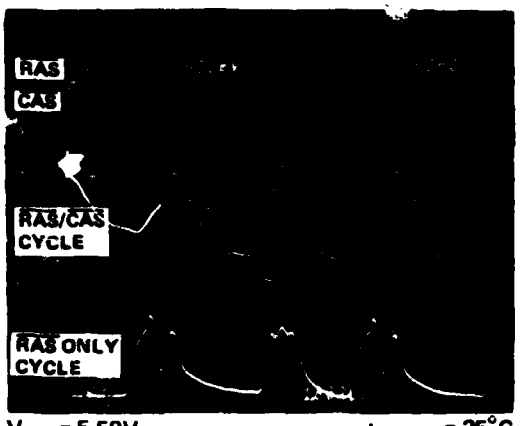


V_{CC} = 5.50V T_{CASE} = -55°C

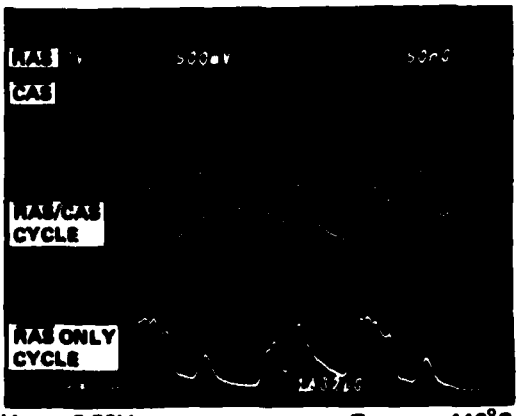


V_{CC} = 5.50V T_{CASE} = -55°C

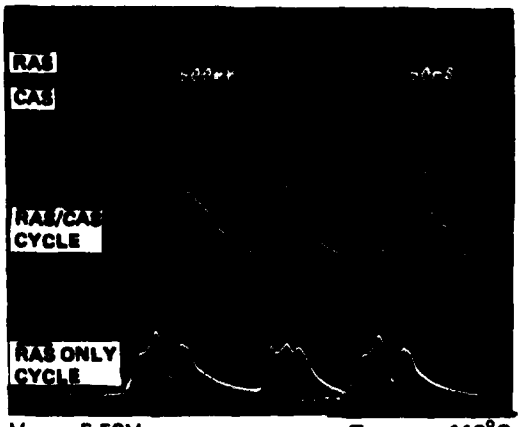
V_{CC} = 5.50V T_{CASE} = 25°C



V_{CC} = 5.50V T_{CASE} = 25°C



V_{CC} = 5.50V T_{CASE} = 110°C

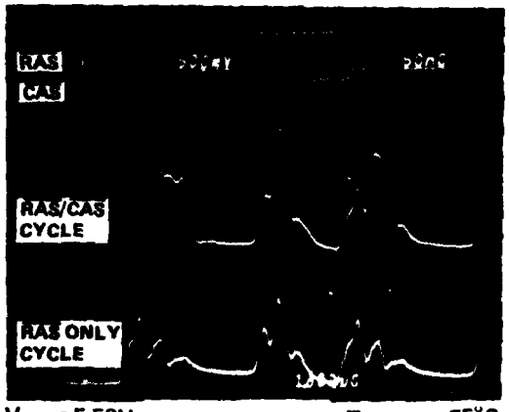


V_{CC} = 5.50V T_{CASE} = 110°C

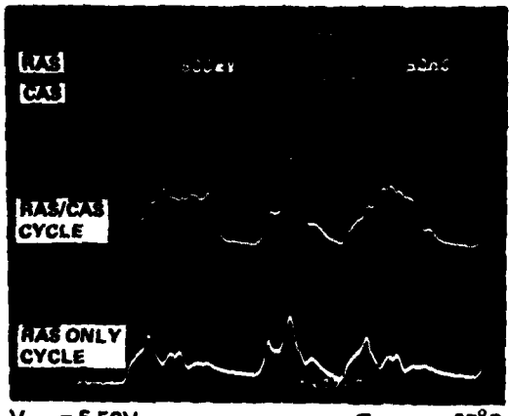
POWER SUPPLY TRANSIENT CURRENT

50 MA/DIV. VERTICAL
50 NS/DIV. HORIZONTAL

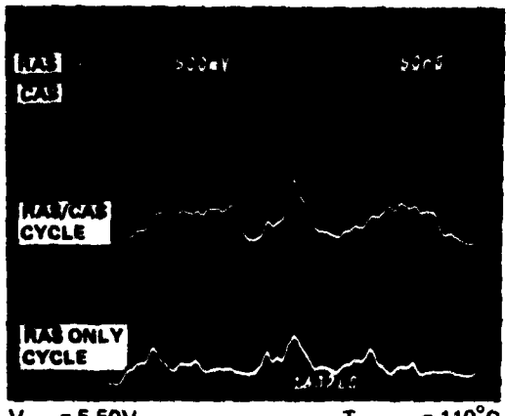
VENDOR C



V_{CC} = 5.50V T_{CASE} = -55°C

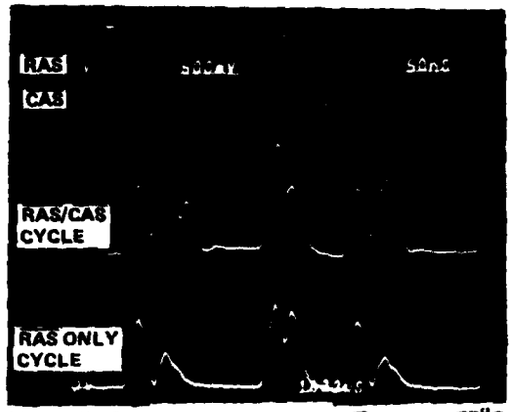


V_{CC} = 5.50V T_{CASE} = 25°C

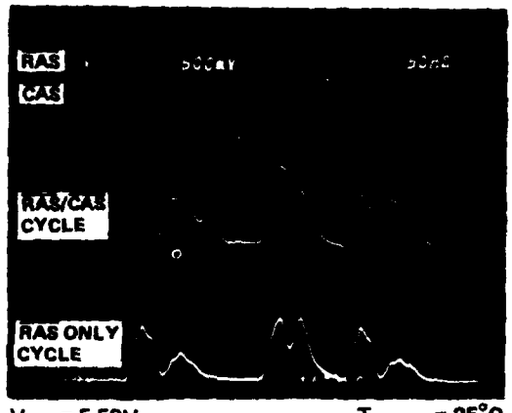


V_{CC} = 5.50V T_{CASE} = 110°C

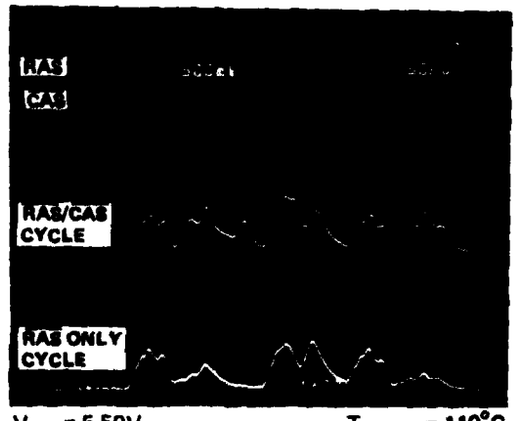
VENDOR D



V_{CC} = 5.50V T_{CASE} = -55°C



V_{CC} = 5.50V T_{CASE} = 25°C



V_{CC} = 5.50V T_{CASE} = 110°C

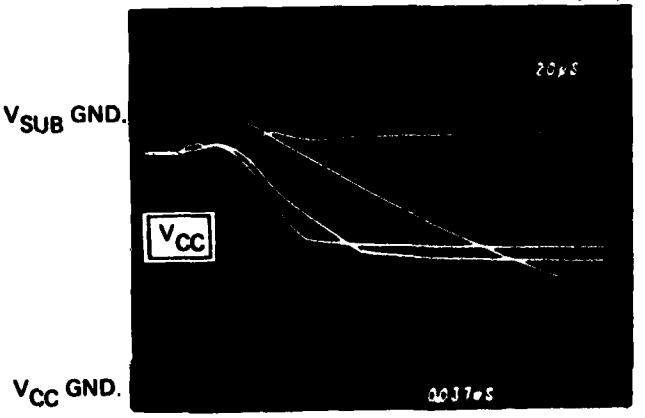
APPENDIX III

SUBSTRATE CHARACTERISTICS

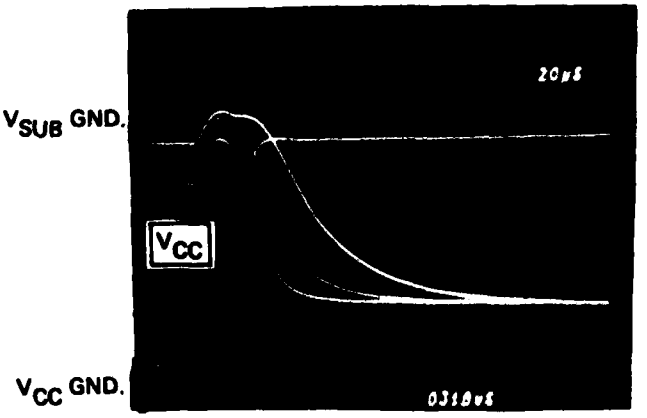
SUBSTRATE TURN-ON TIME

1 V/DIV. VERTICAL
20 μS/DIV. HORIZONTAL

VENDOR A
SUBSTRATE TURN-ON VS. TEMPERATURE (-55, 25, 110°C)

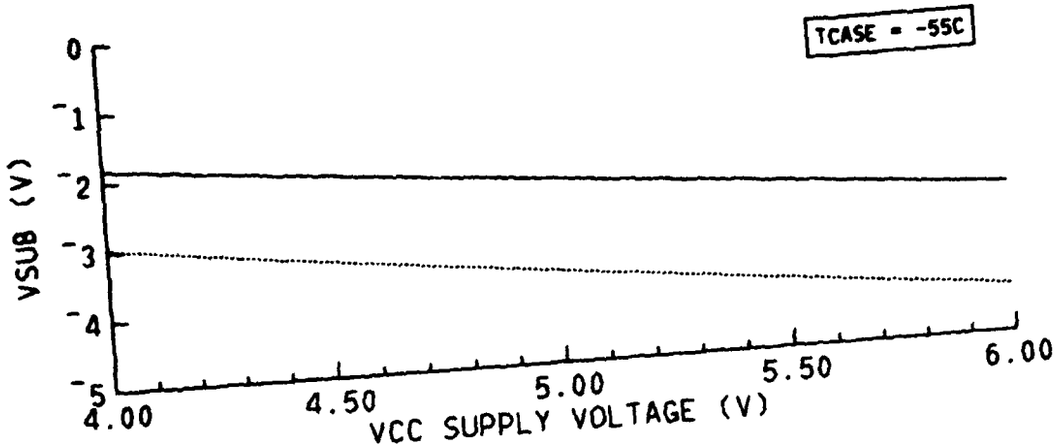


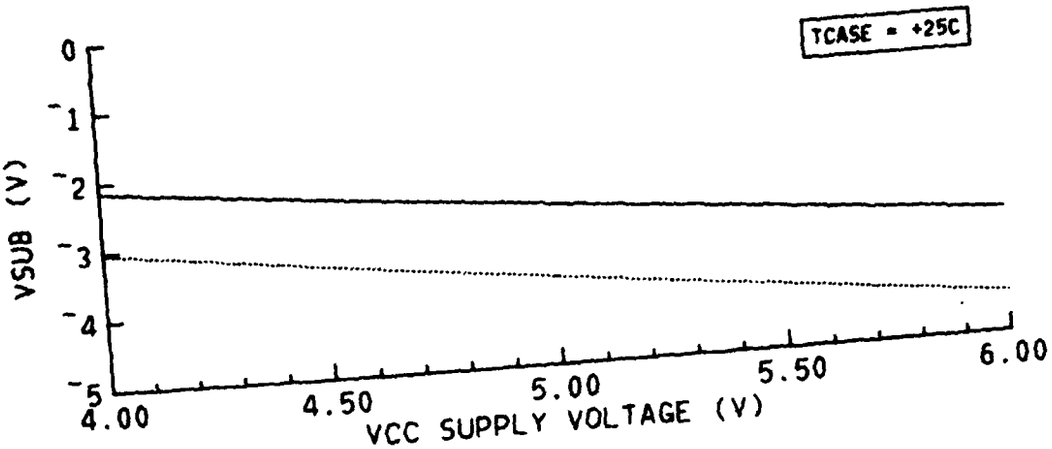
VENDOR B
SUBSTRATE TURN-ON VS. TEMPERATURE (-55, 25, 110°C)

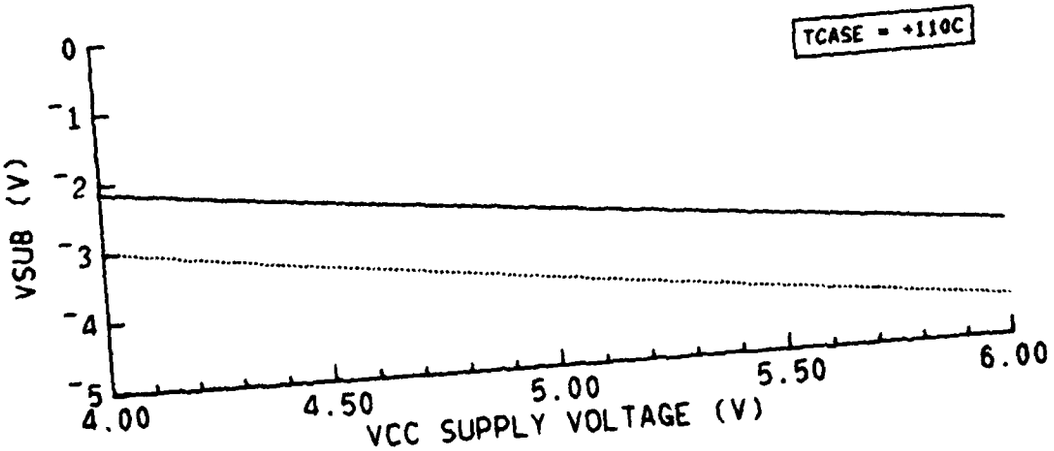


VENDOR A ——
VENDOR B ------

SUBSTRATE VOLTAGE VS SUPPLY VOLTAGE







SCHMOO PLOT: $\overline{\text{RAS}}$ ACCESS TIME (TRAC) VS FORCED SUBSTRATE BIAS (VSUB) VS SUPPLY VOLTAGE (VCC)

VENDOR A

Loose Timing
t_{RC} = 500NS
t_{RAC} = 250NS

T_{CASE}=110°C

VSUB (V)	TRAC (NS)								
1.00	F	F	F	F	F	F	F	F	F
0.50	F	F	F	F	F	F	F	F	F
-0.00	F	F	F	F	F	F	F	F	F
-0.50	F	F	185.0	158.0	144.0	134.0	F	F	F
-1.00	F	201.0	167.0	150.0	139.0	131.0	124.0	119.0	115.0
-1.50	F	189.0	162.0	147.0	136.0	128.0	122.0	117.0	113.0
-2.00	237.0	185.0	160.0	145.0	135.0	127.0	121.0	116.0	112.0
-2.50	236.0	185.0	159.0	145.0	134.0	126.0	120.0	115.0	F
-3.00	240.0	185.0	159.0	144.0	134.0	126.0	120.0	114.0	F
-3.50	F	187.0	160.0	145.0	134.0	126.0	119.0	114.0	F
-4.00	F	189.0	161.0	144.0	134.0	126.0	119.0	114.0	F
-4.50	F	192.0	162.0	145.0	134.0	126.0	119.0	125.0	F
-5.00	F	195.0	163.0	146.0	134.0	126.0	119.0	F	F
-5.50	F	201.0	165.0	147.0	135.0	126.0	119.0	F	F
-6.00	F	216.0	166.0	147.0	135.0	126.0	119.0	F	F
-6.50	F	F	168.0	148.0	136.0	126.0	119.0	F	F
-7.00	F	F	169.0	149.0	136.0	127.0	119.0	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑
	3.00	3.50	4.00	4.50	5.00	5.50	6.00	6.50	7.00

VCC (V)

T_{CASE}=25°C

VSUB (V)	TRAC (NS)								
1.00	F	F	F	F	F	F	F	F	F
0.50	F	F	F	F	F	F	F	F	F
-0.00	F	F	139.0	122.0	114.0	F	F	F	F
-0.50	F	144.0	126.0	115.0	108.0	103.0	99.0	96.0	94.0
-1.00	171.0	138.0	122.0	112.0	106.0	101.0	97.0	94.0	92.0
-1.50	167.0	136.0	120.0	111.0	105.0	100.0	96.0	93.0	90.0
-2.00	168.0	136.0	120.0	110.0	104.0	99.0	95.0	92.0	89.0
-2.50	173.0	137.0	120.0	110.0	103.0	98.0	95.0	91.0	89.0
-3.00	F	139.0	120.0	110.0	103.0	98.0	94.0	90.0	90.0
-3.50	F	140.0	121.0	110.0	103.0	98.0	94.0	90.0	F
-4.00	F	142.0	122.0	110.0	103.0	98.0	94.0	90.0	F
-4.50	F	146.0	123.0	111.0	103.0	98.0	93.0	90.0	F
-5.00	F	156.0	124.0	111.0	103.0	98.0	93.0	90.0	F
-5.50	F	F	125.0	112.0	104.0	98.0	93.0	90.0	F
-6.00	F	F	126.0	112.0	104.0	98.0	93.0	90.0	F
-6.50	F	F	127.0	112.0	104.0	98.0	93.0	94.0	F
-7.00	F	F	128.0	113.0	104.0	98.0	93.0	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑
	3.00	3.50	4.00	4.50	5.00	5.50	6.00	6.50	7.00

VCC (V)

T_{CASE}=-55°C

VSUB (V)	TRAC (NS)								
1.00	F	F	F	F	F	F	F	F	F
0.50	F	F	109.0	98.0	92.0	88.0	85.0	83.0	81.0
-0.00	F	110.0	99.0	92.0	88.0	85.0	82.0	80.0	79.0
-0.50	124.0	105.0	95.0	89.0	85.0	82.0	80.0	78.0	77.0
-1.00	122.0	104.0	94.0	88.0	84.0	81.0	79.0	77.0	75.0
-1.50	123.0	104.0	93.0	87.0	83.0	80.0	77.0	76.0	74.0
-2.00	F	104.0	93.0	86.0	82.0	79.0	77.0	75.0	74.0
-2.50	F	105.0	93.0	86.0	82.0	79.0	76.0	75.0	74.0
-3.00	F	F	93.0	86.0	81.0	78.0	76.0	74.0	73.0
-3.50	F	F	94.0	86.0	81.0	77.0	75.0	74.0	73.0
-4.00	F	F	94.0	86.0	81.0	78.0	75.0	74.0	73.0
-4.50	F	F	95.0	86.0	81.0	77.0	75.0	74.0	72.0
-5.00	F	F	96.0	86.0	81.0	77.0	75.0	73.0	72.0
-5.50	F	F	125.0	87.0	81.0	77.0	75.0	73.0	72.0
-6.00	F	F	F	87.0	81.0	77.0	75.0	73.0	72.0
-6.50	F	F	F	87.0	82.0	77.0	75.0	73.0	F
-7.00	F	F	F	88.0	82.0	78.0	75.0	73.0	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑
	3.00	3.50	4.00	4.50	5.00	5.50	6.00	6.50	7.00

VCC (V)

SCHMOO PLOT: $\overline{RAS}$ ACCESS TIME (TRAC) VS FORCED SUBSTRATE BIAS (VSUB) VS SUPPLY VOLTAGE (VCC)

VENDOR B

Loose Timing
t_{RC} = 500NS
t_{RAC} = 250NS

T_{CASE}=+110°C

VSUB (V) TRAC (NS)

1.00	F	F	F	F	F	F	F	F	F
0.50	F	F	F	F	F	F	F	F	F
-0.00	F	F	F	F	F	F	F	F	F
-0.50	F	186.0	155.0	136.0	124.0	114.0	107.0	103.0	F
-1.00	F	183.0	154.0	136.0	123.0	114.0	107.0	102.0	F
-1.50	F	183.0	154.0	136.0	123.0	114.0	107.0	102.0	F
-2.00	F	184.0	155.0	136.0	124.0	114.0	107.0	102.0	F
-2.50	F	186.0	156.0	137.0	124.0	114.0	107.0	102.0	F
-3.00	F	188.0	158.0	138.0	125.0	115.0	108.0	102.0	F
-3.50	F	191.0	160.0	140.0	126.0	115.0	108.0	103.0	F
-4.00	F	195.0	162.0	141.0	127.0	116.0	109.0	103.0	F
-4.50	F	198.0	164.0	143.0	128.0	117.0	109.0	104.0	F
-5.00	F	202.0	166.0	144.0	129.0	118.0	110.0	104.0	F
-5.50	F	206.0	168.0	146.0	130.0	119.0	111.0	105.0	F
-6.00	F	210.0	171.0	147.0	131.0	120.0	111.0	105.0	F
-6.50	F	215.0	174.0	149.0	133.0	121.0	112.0	105.0	F
-7.00	F	220.0	176.0	151.0	134.0	122.0	113.0	106.0	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑
	3.00	3.50	4.00	4.50	5.00	5.50	6.00	6.50	7.00

VCC (V)

T_{CASE}=+25°C

VSUB (V) TRAC (NS)

1.00	F	F	F	F	F	F	F	F	
0.50	F	F	F	F	F	F	F	F	
-0.00	F	132.0	112.0	102.0	96.0	91.0	86.0	84.0	
-0.50	F	129.0	111.0	101.0	95.0	90.0	86.0	83.0	
-1.00	F	129.0	111.0	101.0	95.0	90.0	86.0	83.0	
-1.50	F	130.0	112.0	102.0	95.0	90.0	86.0	83.0	
-2.00	F	132.0	112.0	102.0	96.0	91.0	86.0	83.0	
-2.50	F	134.0	114.0	102.0	96.0	91.0	87.0	83.0	
-3.00	F	136.0	115.0	103.0	96.0	91.0	87.0	84.0	
-3.50	F	138.0	116.0	104.0	97.0	92.0	87.0	84.0	
-4.00	F	141.0	117.0	104.0	97.0	92.0	87.0	84.0	
-4.50	F	144.0	119.0	105.0	97.0	92.0	88.0	84.0	
-5.00	F	146.0	121.0	106.0	98.0	93.0	88.0	84.0	
-5.50	F	149.0	122.0	107.0	98.0	93.0	88.0	85.0	
-6.00	F	153.0	124.0	108.0	99.0	94.0	89.0	85.0	
-6.50	F	156.0	126.0	109.0	99.0	94.0	89.0	85.0	
-7.00	F	159.0	128.0	110.0	100.0	94.0	89.0	85.0	
	↑	↑	↑	↑	↑	↑	↑	↑	↑
	3.00	3.50	4.00	4.50	5.00	5.50	6.00	6.50	

VCC (V)

T_{CASE}=-55°C

VSUB (V) TRAC (NS)

1.00	F	F	F	F	F	F	F	F	F
0.50	F	F	F	F	F	F	F	F	F
-0.00	F	99.0	89.0	82.0	78.0	75.0	74.0	72.0	72.0
-0.50	F	100.0	89.0	82.0	78.0	75.0	74.0	72.0	F
-1.00	F	100.0	90.0	83.0	78.0	75.0	74.0	72.0	F
-1.50	F	101.0	90.0	83.0	78.0	75.0	74.0	72.0	72.0
-2.00	F	102.0	91.0	83.0	79.0	75.0	74.0	72.0	71.0
-2.50	F	103.0	92.0	84.0	79.0	75.0	74.0	72.0	F
-3.00	F	104.0	93.0	84.0	79.0	76.0	74.0	72.0	F
-3.50	F	104.0	94.0	85.0	79.0	76.0	74.0	73.0	F
-4.00	F	105.0	95.0	85.0	80.0	76.0	74.0	72.0	F
-4.50	F	107.0	95.0	86.0	80.0	76.0	74.0	73.0	F
-5.00	F	108.0	96.0	87.0	80.0	76.0	74.0	73.0	F
-5.50	F	110.0	97.0	87.0	81.0	77.0	74.0	73.0	F
-6.00	F	112.0	98.0	88.0	81.0	77.0	74.0	73.0	F
-6.50	F	114.0	99.0	89.0	82.0	77.0	75.0	73.0	F
-7.00	F	115.0	99.0	89.0	82.0	77.0	75.0	73.0	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑
	3.00	3.50	4.00	4.50	5.00	5.50	6.00	6.50	7.00

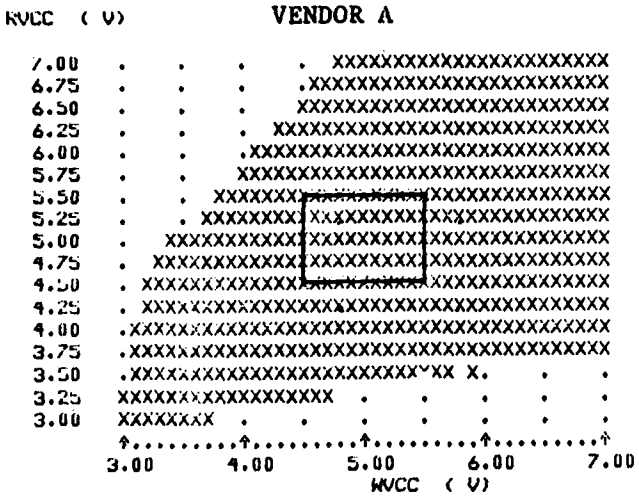
VCC (V)

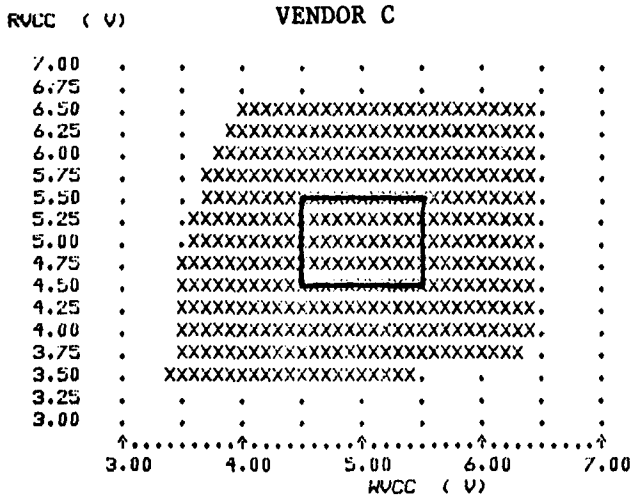
APPENDIX IV

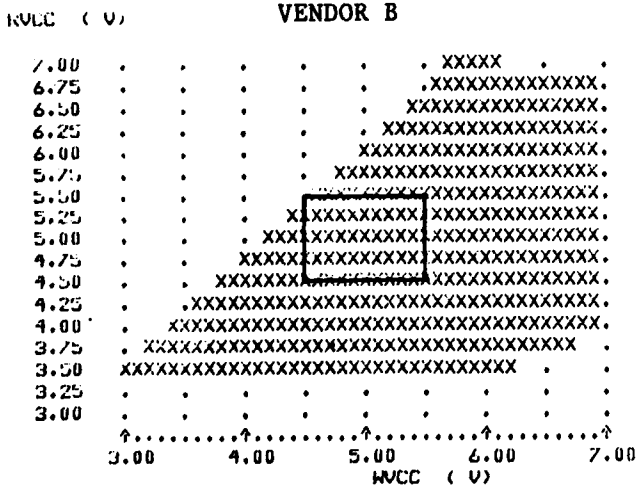
BUMP VOLTAGE SCHMOOS (VCC SLEW TEST)

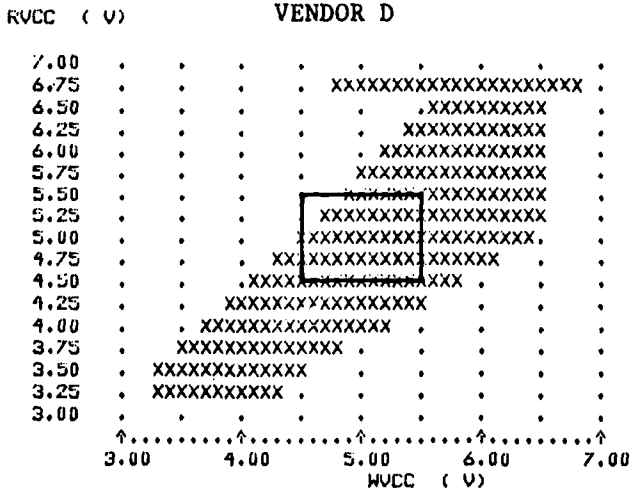
SCHMOO PLOT: VOLTAGE BUMP-READ CYCLE VCC (RVCC) VS WRITE CYCLE VCC (WVCC)

$T_{CASE} = -55^{o}C$





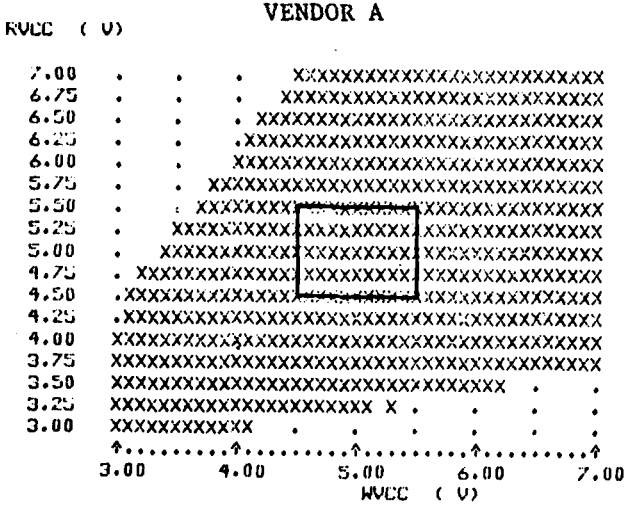




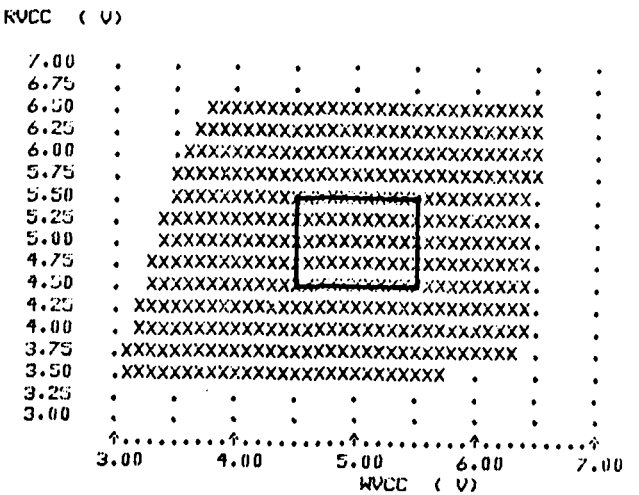
SCHMOO PLOT: VOLTAGE BUMP-READ CYCLE (RVCC) VS WRITE CYCLE (WVCC)

T_{CASE} = 25°C

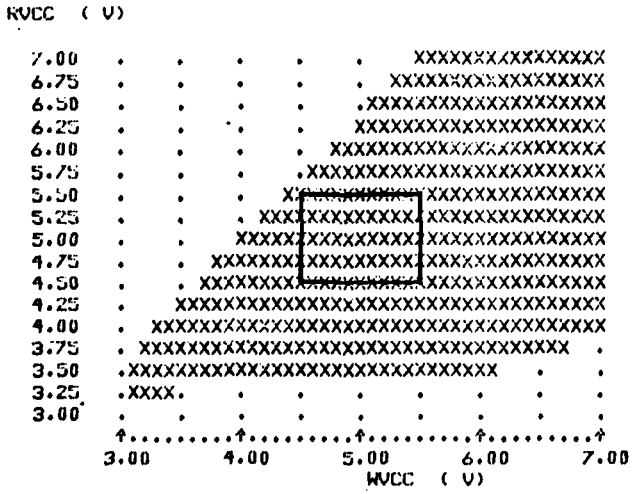
VENDOR A



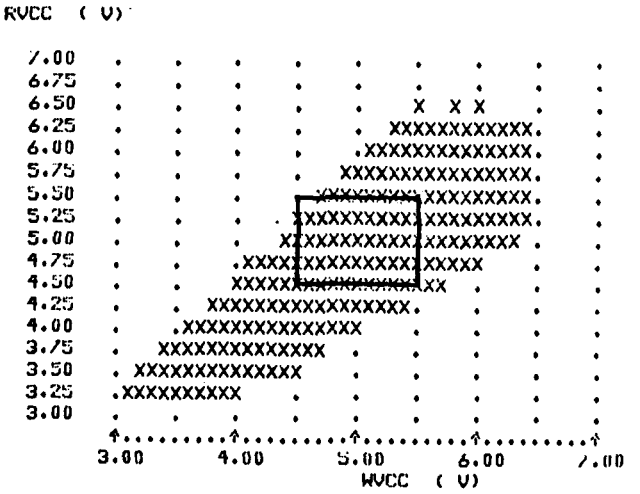
VENDOR C



VENDOR B



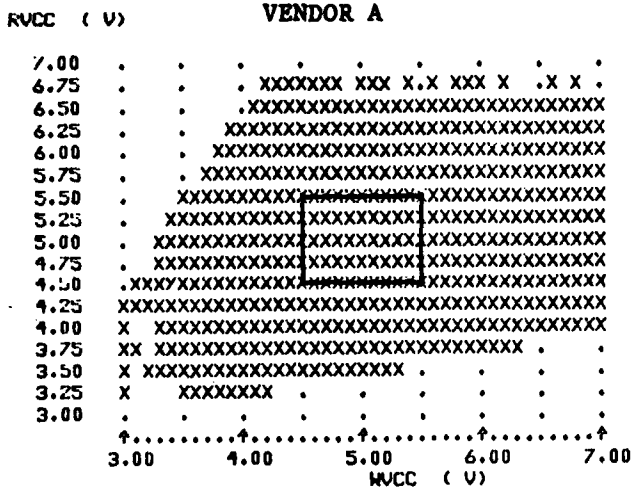
VENDOR D



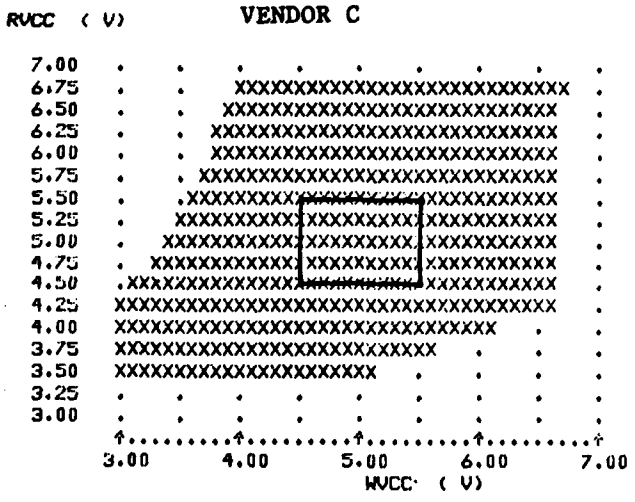
SCHMOO PLOT: VOLTAGE BUMP-READ CYCLE VCC (RVCC) VS WRITE CYCLE VCC (WVCC)

T_{CASE} = +110°C

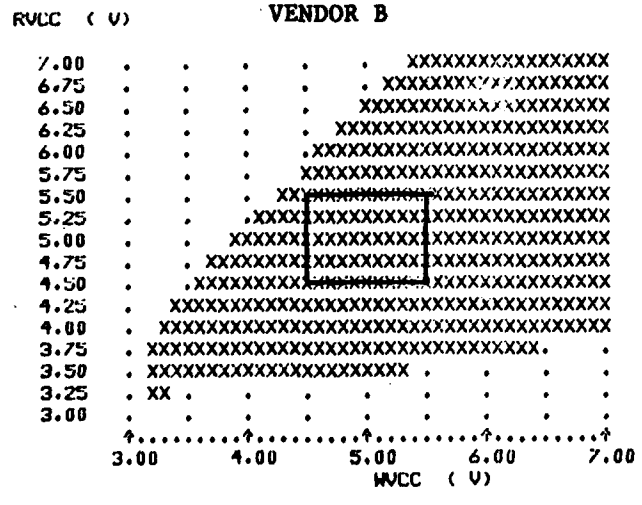
VENDOR A



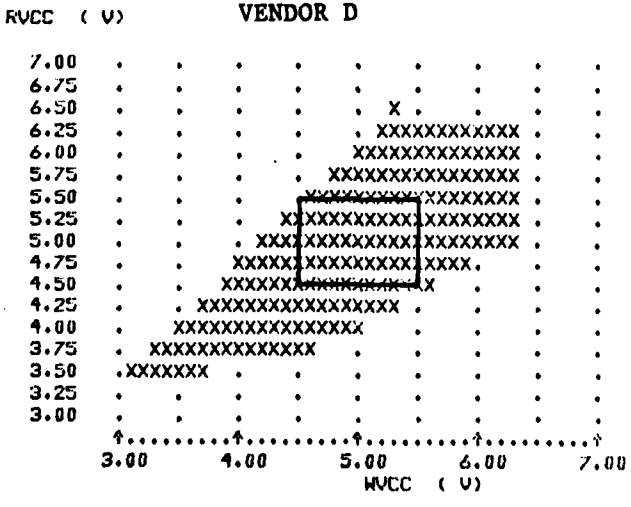
VENDOR C



VENDOR B



VENDOR D



APPENDIX V

$\overline{\text{RAS}}$ TO $\overline{\text{CAS}}$ DELAY SCHMOOS

SCHMOO PLOT: ACCESS TIME FROM $\overline{RAS}$ (TRAC) VS SUPPLY VOLTAGE (VCC) VS $\overline{RAS}$ TO $\overline{CAS}$ DELAY (TRCD)

VENDOR A

$T_{CASE} = +110^{\circ}C$

VCC (V)	TRAC (NS)										
6.50	F	F	F	F	F	F	F	F	F	F	F
6.25	120.0	120.0	120.0	120.0	120.0	125.0	134.0	144.0	153.0	163.0	173.0
6.00	124.0	124.0	124.0	124.0	124.0	127.0	137.0	146.0	156.0	165.0	175.0
5.75	129.0	129.0	129.0	129.0	129.0	131.0	140.0	149.0	158.0	168.0	178.0
5.50	134.0	134.0	134.0	134.0	134.0	135.0	143.0	152.0	162.0	171.0	181.0
5.25	140.0	140.0	140.0	140.0	140.0	140.0	147.0	156.0	165.0	175.0	185.0
5.00	147.0	147.0	147.0	147.0	147.0	147.0	151.0	160.0	169.0	179.0	189.0
4.75	155.0	155.0	155.0	155.0	155.0	155.0	156.0	165.0	174.0	184.0	193.0
4.50	165.0	165.0	165.0	165.0	165.0	165.0	165.0	171.0	180.0	189.0	199.0
4.25	175.0	175.0	175.0	175.0	175.0	175.0	176.0	178.0	186.0	196.0	205.0
4.00	189.0	188.0	189.0	189.0	189.0	189.0	189.0	189.0	195.0	204.0	213.0
3.75	205.0	205.0	205.0	205.0	205.0	205.0	205.0	205.0	206.0	214.0	223.0
3.50	230.0	230.0	230.0	230.0	230.0	230.0	230.0	230.0	231.0	232.0	241.0
3.25	F	F	F	F	F	F	F	F	F	F	F
3.00	F	F	F	F	F	F	F	F	F	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0

TRCD (NS)

$T_{CASE} = -55^{\circ}C$

VCC (V)	TRAC (NS)										
6.50	F	F	F	68.0	77.0	87.0	97.0	107.0	117.0	127.0	137.0
6.25	F	F	F	69.0	78.0	88.0	98.0	108.0	118.0	127.0	138.0
6.00	65.0	65.0	65.0	70.0	79.0	89.0	99.0	109.0	119.0	129.0	139.0
5.75	67.0	67.0	67.0	72.0	81.0	91.0	100.0	110.0	120.0	130.0	140.0
5.50	70.0	70.0	70.0	74.0	82.0	92.0	102.0	112.0	122.0	132.0	142.0
5.25	74.0	73.0	73.0	75.0	[illegible].0	94.0	104.0	114.0	124.0	134.0	144.0
5.00	77.0	77.0	77.0	78.0	87.0	96.0	106.0	116.0	126.0	136.0	146.0
4.75	82.0	81.0	81.0	82.0	90.0	99.0	109.0	119.0	129.0	139.0	149.0
4.50	87.0	86.0	86.0	86.0	93.0	102.0	111.0	122.0	132.0	142.0	152.0
4.25	93.0	93.0	93.0	93.0	97.0	106.0	115.0	125.0	135.0	145.0	155.0
4.00	100.0	100.0	100.0	100.0	101.0	111.0	120.0	130.0	140.0	150.0	160.0
3.75	110.0	110.0	110.0	110.0	110.0	116.0	127.0	136.0	146.0	156.0	166.0
3.50	125.0	125.0	125.0	125.0	125.0	128.0	137.0	147.0	156.0	166.0	176.0
3.25	149.0	149.0	149.0	149.0	149.0	149.0	154.0	164.0	173.0	183.0	192.0
3.00	F	F	F	F	F	F	F	F	F	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0

TRCD (NS)

Loose Timing

t_{RC} = 500NS

t_{RAC} = 250NS

SCHMOO PLOT: ACCESS TIME FROM $\overline{RAS}$ (TRAC) VS SUPPLY VOLTAGE (VCC) VS $\overline{RAS}$ TO $\overline{CAS}$ DELAY (TRCD)

VENDOR B

$T_{CASE} = +110^{\circ}C$

VCC (V)	TRAC (NS)										
6.50	F	F	F	104.0	106.0	113.0	122.0	132.0	141.0	151.0	161.0
6.25	F	F	107.0	107.0	108.0	114.0	123.0	132.0	142.0	152.0	162.0
6.00	110.0	110.0	110.0	110.0	111.0	116.0	125.0	134.0	144.0	154.0	164.0
5.75	113.0	114.0	113.0	114.0	115.0	119.0	127.0	136.0	146.0	156.0	166.0
5.50	117.0	117.0	117.0	117.0	118.0	122.0	130.0	139.0	148.0	158.0	168.0
5.25	122.0	121.0	122.0	122.0	122.0	125.0	132.0	141.0	151.0	160.0	170.0
5.00	127.0	127.0	127.0	127.0	127.0	129.0	135.0	144.0	154.0	163.0	173.0
4.75	133.0	133.0	133.0	133.0	134.0	135.0	140.0	148.0	157.0	167.0	177.0
4.50	141.0	141.0	141.0	141.0	141.0	142.0	145.0	154.0	162.0	172.0	181.0
4.25	150.0	150.0	150.0	150.0	150.0	151.0	153.0	160.0	168.0	177.0	187.0
4.00	162.0	162.0	163.0	162.0	162.0	162.0	164.0	168.0	176.0	185.0	194.0
3.75	178.0	178.0	179.0	178.0	178.0	178.0	178.0	180.0	187.0	195.0	204.0
3.50	201.0	201.0	201.0	202.0	202.0	201.0	200.0	201.0	204.0	211.0	220.0
3.25	F	F	F	F	F	F	F	F	F	F	F
3.00	F	F	F	F	F	F	F	F	F	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0
	TRCD (NS)										

$T_{CASE} = -55^{\circ}C$

VCC (V)	TRAC (NS)										
6.50	F	F	F	F	F	203.0	94.0	104.0	114.0	124.0	134.0
6.25	F	F	F	F	75.0	85.0	95.0	105.0	115.0	125.0	135.0
6.00	F	F	F	66.0	75.0	85.0	95.0	105.0	115.0	125.0	135.0
5.75	F	F	F	67.0	76.0	86.0	96.0	106.0	116.0	125.0	136.0
5.50	F	F	F	68.0	77.0	87.0	97.0	107.0	117.0	127.0	137.0
5.25	F	F	F	69.0	78.0	89.0	99.0	109.0	119.0	129.0	139.0
5.00	F	F	F	71.0	80.0	90.0	100.0	110.0	120.0	130.0	140.0
4.75	F	F	F	74.0	82.0	92.0	102.0	112.0	122.0	132.0	142.0
4.50	F	F	F	76.0	85.0	95.0	105.0	115.0	125.0	135.0	145.0
4.25	F	F	F	79.0	87.0	97.0	107.0	117.0	127.0	137.0	147.0
4.00	F	F	F	82.0	91.0	100.0	110.0	121.0	131.0	141.0	151.0
3.75	F	F	F	87.0	95.0	105.0	115.0	125.0	135.0	145.0	155.0
3.50	F	F	F	94.0	102.0	111.0	121.0	131.0	141.0	151.0	161.0
3.25	F	F	F	F	F	F	F	F	F	F	F
3.00	F	F	F	F	F	F	F	F	F	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0
	TRCD (NS)										

Loose Timing

t_{RC} = 500NS

t_{RAC} = 250NS

SCHMOO PLOT: ACCESS TIME FROM $\overline{RAS}$ (TRAC) VS SUPPLY VOLTAGE (VCC) VS $\overline{RAS}$ TO $\overline{CAS}$ DELAY (TRCD)

VENDOR C

T_{CASE} = +110°C

VCC (V)	TRAC (NS)										
6.50	104.0	104.0	104.0	104.0	105.0	110.0	118.0	128.0	138.0	148.0	157.0
6.25	107.0	107.0	107.0	107.0	107.0	112.0	120.0	130.0	140.0	150.0	159.0
6.00	110.0	110.0	110.0	110.0	110.0	115.0	123.0	132.0	142.0	152.0	162.0
5.75	113.0	113.0	113.0	113.0	113.0	117.0	125.0	134.0	144.0	154.0	164.0
5.50	117.0	117.0	117.0	117.0	117.0	121.0	128.0	137.0	147.0	157.0	167.0
5.25	122.0	122.0	122.0	122.0	122.0	125.0	132.0	141.0	150.0	160.0	170.0
5.00	127.0	127.0	127.0	127.0	127.0	129.0	136.0	145.0	154.0	164.0	174.0
4.75	133.0	133.0	133.0	133.0	133.0	134.0	141.0	149.0	158.0	168.0	177.0
4.50	140.0	140.0	139.0	139.0	139.0	139.0	146.0	154.0	163.0	173.0	182.0
4.25	147.0	147.0	147.0	147.0	147.0	147.0	152.0	161.0	169.0	179.0	188.0
4.00	157.0	157.0	157.0	157.0	157.0	157.0	160.0	169.0	177.0	186.0	195.0
3.75	169.0	169.0	169.0	169.0	169.0	169.0	170.0	178.0	186.0	195.0	204.0
3.50	185.0	185.0	185.0	185.0	185.0	185.0	185.0	190.0	200.0	207.0	216.0
3.25	216.0	216.0	216.0	216.0	215.0	215.0	216.0	217.0	225.0	234.0	242.0
3.00	F	F	F	F	F	F	F	F	F	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0
	TRCD (NS)										

T_{CASE} = -55°C

VCC (V)	TRAC (NS)										
6.50	F	F	F	63.0	73.0	82.0	92.0	102.0	112.0	122.0	132.0
6.25	F	F	F	64.0	73.0	83.0	93.0	103.0	113.0	123.0	133.0
6.00	F	F	F	65.0	74.0	84.0	94.0	104.0	114.0	124.0	134.0
5.75	F	F	F	67.0	75.0	85.0	95.0	105.0	115.0	125.0	135.0
5.50	64.0	64.0	64.0	68.0	76.0	86.0	96.0	106.0	116.0	126.0	136.0
5.25	66.0	66.0	65.0	70.0	77.0	88.0	97.0	107.0	117.0	127.0	137.0
5.00	68.0	68.0	68.0	72.0	79.0	89.0	99.0	109.0	119.0	129.0	139.0
4.75	71.0	71.0	71.0	74.0	82.0	92.0	101.0	111.0	121.0	131.0	141.0
4.50	74.0	74.0	74.0	76.0	84.0	94.0	104.0	114.0	124.0	134.0	144.0
4.25	78.0	78.0	78.0	79.0	87.0	97.0	107.0	116.0	126.0	136.0	146.0
4.00	82.0	82.0	82.0	83.0	92.0	100.0	110.0	120.0	130.0	140.0	150.0
3.75	88.0	88.0	88.0	88.0	97.0	105.0	115.0	124.0	134.0	144.0	154.0
3.50	95.0	95.0	95.0	95.0	103.0	111.0	120.0	130.0	139.0	149.0	159.0
3.25	F	F	F	F	F	F	F	F	F	F	F
3.00	F	F	F	F	F	F	F	F	F	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0
	TRCD (NS)										

Loose Timing

t_{RC} = 500NS

t_{RAC} = 250NS

SCHMOO PLOT: ACCESS TIME FROM $\overline{RAS}$ (TRAC) VS SUPPLY VOLTAGE (VCC)
VS $\overline{RAS}$ TO $\overline{CAS}$ DELAY (TRCD)
VENDOR D

T_{CASE} = +110°C

VCC (V)	TRAC (NS)										
6.50	F	F	F	F	F	F	116.0	122.0	131.0	141.0	151.0
6.25	117.0	117.0	117.0	117.0	117.0	117.0	117.0	124.0	133.0	143.0	153.0
6.00	120.0	120.0	120.0	120.0	120.0	120.0	120.0	127.0	136.0	145.0	155.0
5.75	123.0	123.0	123.0	123.0	123.0	123.0	124.0	129.0	138.0	147.0	157.0
5.50	127.0	127.0	127.0	127.0	127.0	127.0	127.0	131.0	140.0	149.0	159.0
5.25	130.0	130.0	130.0	130.0	130.0	130.0	130.0	133.0	142.0	151.0	162.0
5.00	135.0	135.0	135.0	135.0	135.0	135.0	135.0	136.0	145.0	154.0	164.0
4.75	140.0	140.0	140.0	140.0	140.0	140.0	140.0	140.0	148.0	157.0	167.0
4.50	145.0	145.0	145.0	145.0	145.0	145.0	145.0	145.0	152.0	161.0	170.0
4.25	152.0	152.0	152.0	152.0	152.0	152.0	152.0	152.0	155.0	165.0	174.0
4.00	160.0	160.0	160.0	160.0	160.0	160.0	160.0	160.0	161.0	170.0	179.0
3.75	172.0	171.0	172.0	172.0	172.0	172.0	172.0	172.0	172.0	177.0	186.0
3.50	186.0	186.0	186.0	186.0	186.0	186.0	186.0	186.0	186.0	187.0	195.0
3.25	207.0	207.0	208.0	207.0	207.0	207.0	207.0	207.0	207.0	207.0	209.0
3.00	243.0	242.0	242.0	243.0	243.0	243.0	243.0	243.0	244.0	243.0	243.0
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0
	TRCD (NS)										

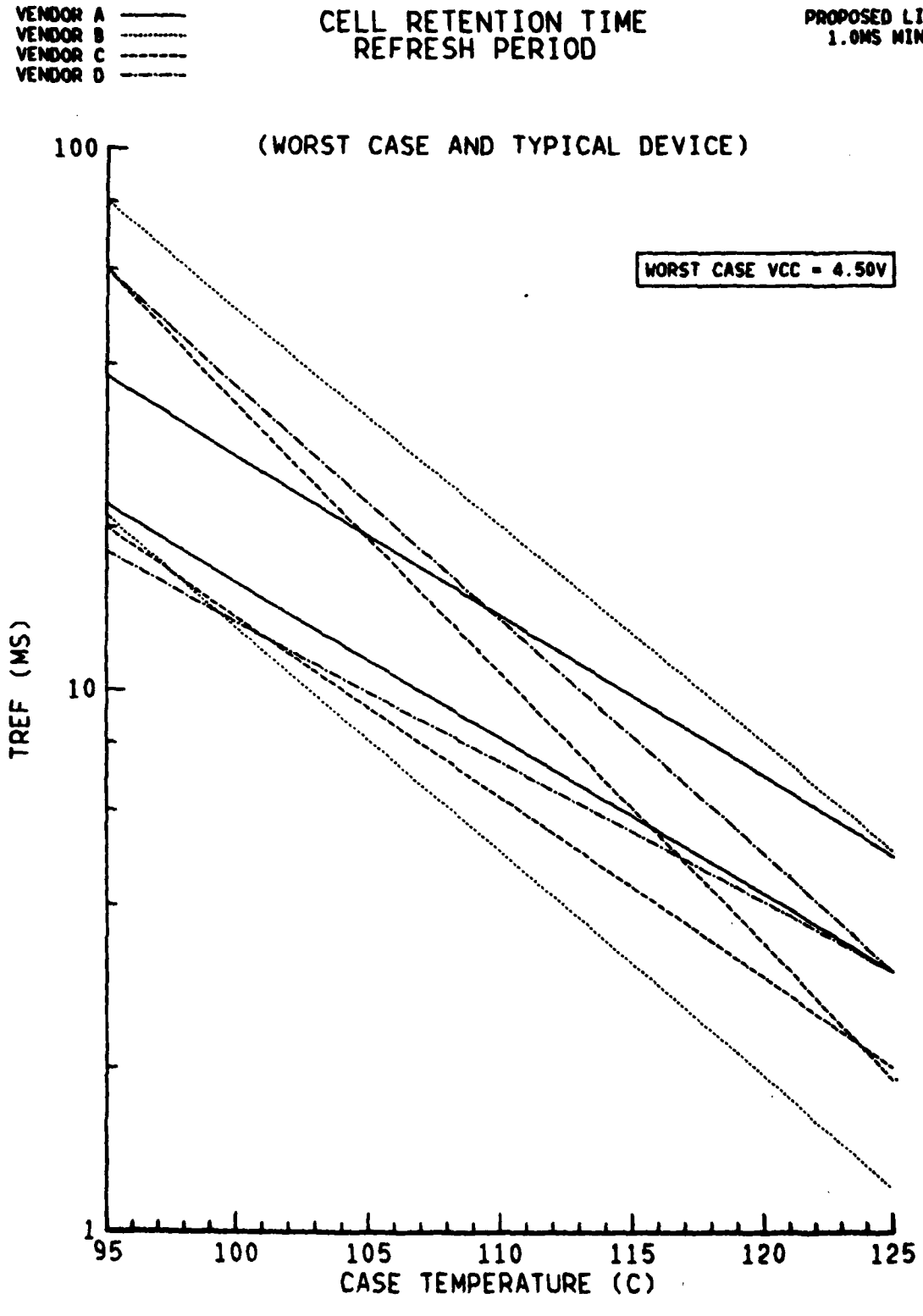
T_{CASE} = -55°C

VCC (V)	TRAC (NS)										
6.50	74.0	74.0	74.0	74.0	74.0	82.0	91.0	102.0	111.0	122.0	131.0
6.25	75.0	75.0	75.0	75.0	75.0	83.0	92.0	102.0	112.0	122.0	132.0
6.00	76.0	76.0	76.0	76.0	76.0	84.0	92.0	103.0	113.0	123.0	133.0
5.75	77.0	77.0	77.0	77.0	77.0	84.0	93.0	104.0	114.0	124.0	134.0
5.50	79.0	79.0	79.0	79.0	79.0	85.0	94.0	105.0	115.0	125.0	135.0
5.25	80.0	80.0	80.0	80.0	80.0	86.0	95.0	105.0	115.0	125.0	135.0
5.00	82.0	82.0	82.0	82.0	82.0	87.0	96.0	106.0	116.0	126.0	136.0
4.75	84.0	84.0	84.0	84.0	84.0	88.0	97.0	107.0	117.0	127.0	137.0
4.50	86.0	86.0	86.0	86.0	86.0	89.0	98.0	109.0	119.0	129.0	139.0
4.25	89.0	89.0	89.0	89.0	89.0	91.0	101.0	111.0	121.0	131.0	141.0
4.00	93.0	93.0	93.0	93.0	93.0	94.0	103.0	113.0	123.0	133.0	143.0
3.75	97.0	98.0	98.0	98.0	98.0	98.0	106.0	115.0	126.0	136.0	145.0
3.50	104.0	104.0	104.0	104.0	104.0	104.0	110.0	118.0	129.0	139.0	149.0
3.25	112.0	112.0	112.0	112.0	112.0	112.0	115.0	124.0	133.0	144.0	154.0
3.00	F	F	F	F	F	F	124.0	141.0	F	F	F
	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0
	TRCD (NS)										

Loose Timing
t_{RC} = 500NS
t_{RAC} = 250NS

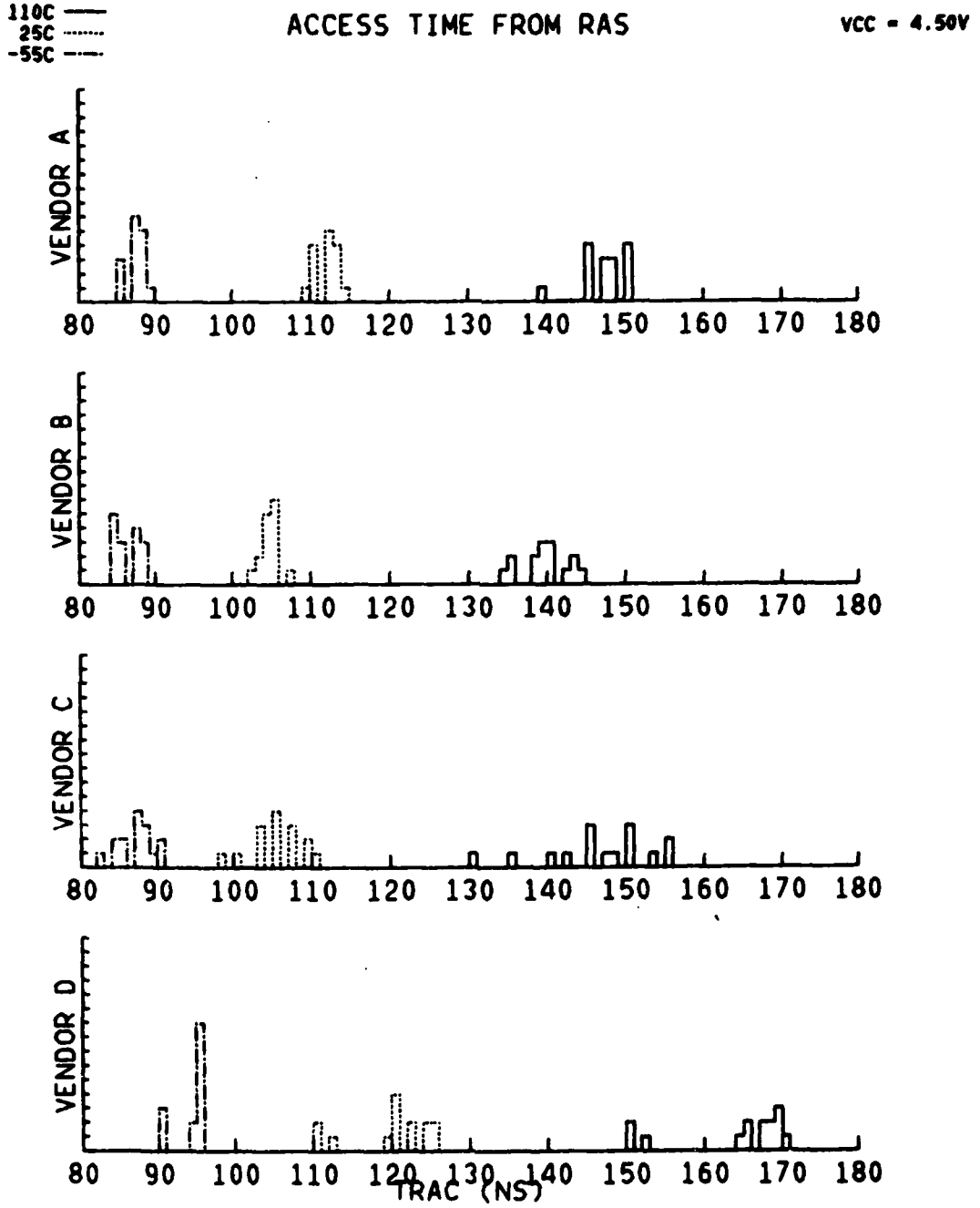
APPENDIX VI

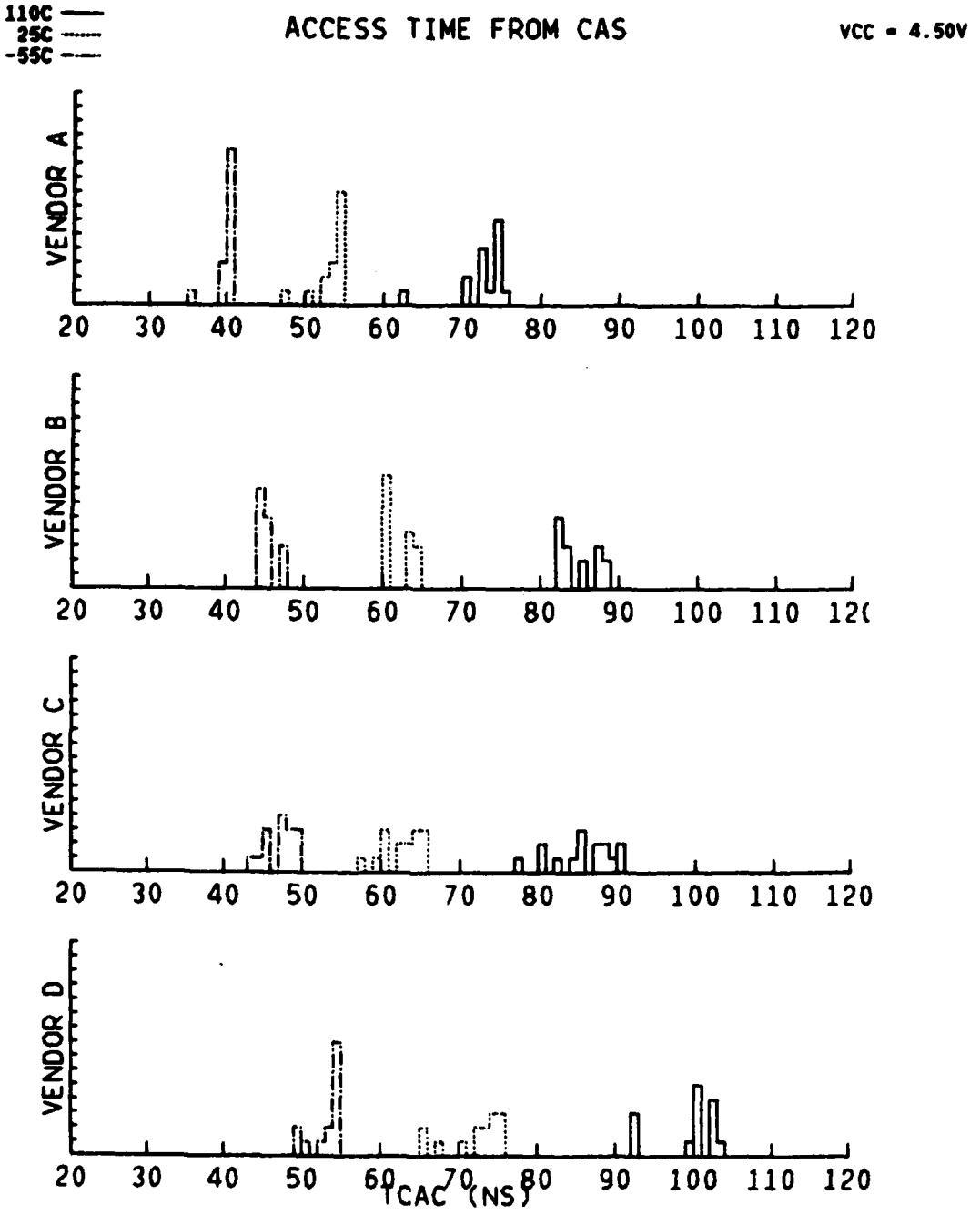
CELL RETENTION TIME GRAPH

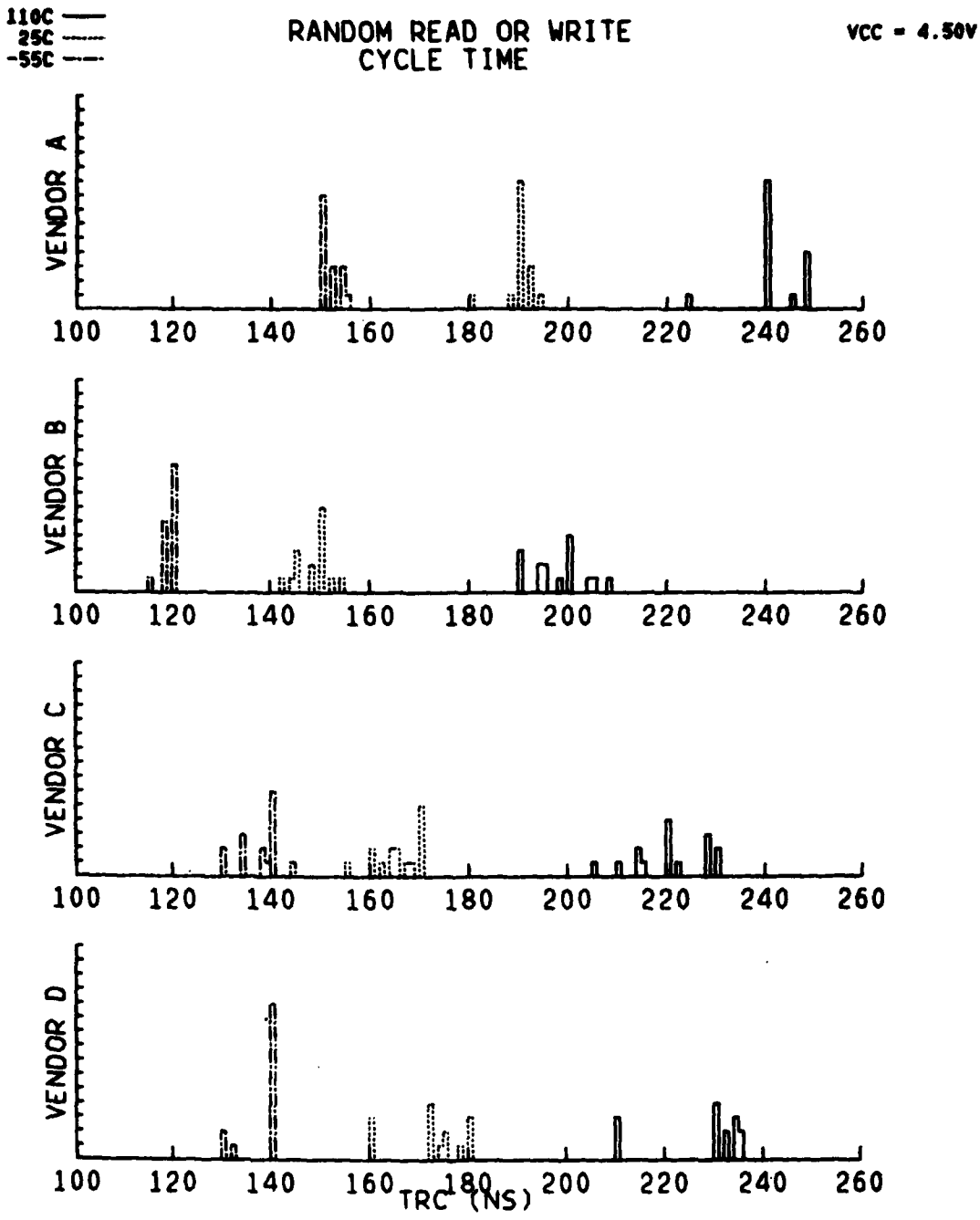

VENDOR A
VENDOR B
VENDOR C
VENDOR D
CELL RETENTION TIME
REFRESH PERIOD
PROPOSED LIMIT
1.0MS MIN
(WORST CASE AND TYPICAL DEVICE)
WORST CASE VCC = 4.50V
100
10
1
TREF (MS)
95
100
105
110
115
120
125
CASE TEMPERATURE (C)

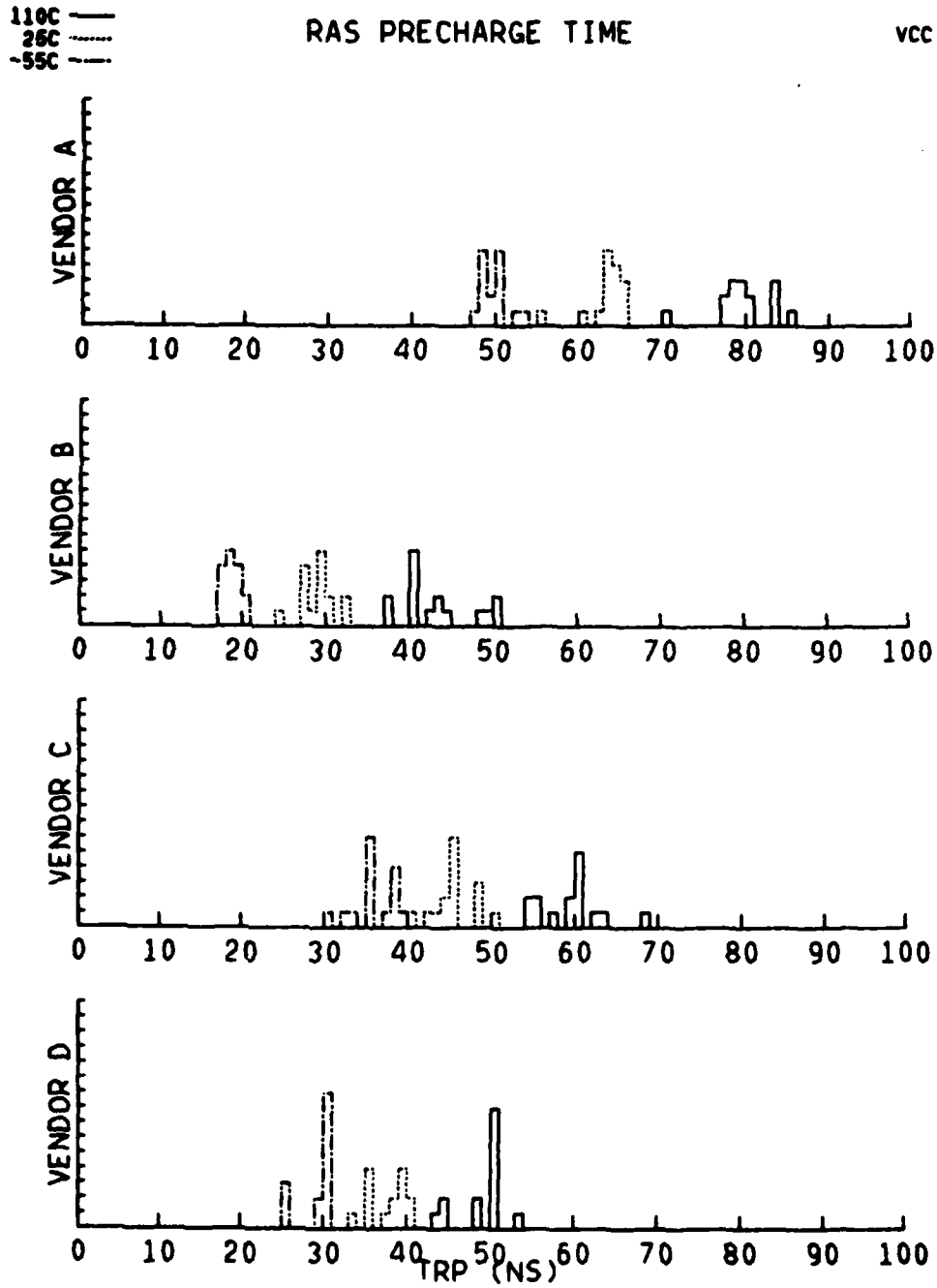
APPENDIX VII

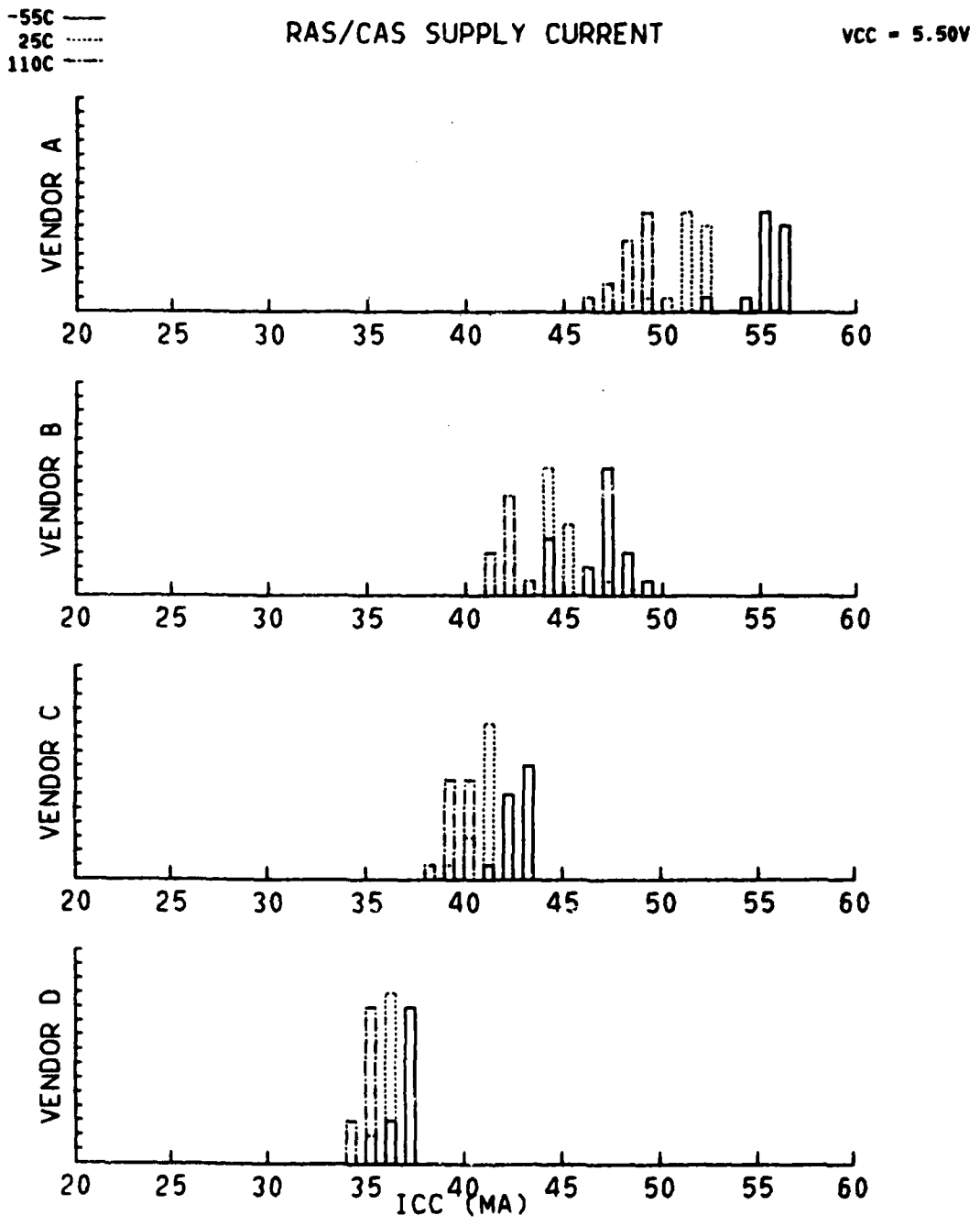
HISTOGRAMS


110C
25C
-55C
ACCESS TIME FROM RAS
VCC = 4.50V
VENDOR A
VENDOR B
VENDOR C
VENDOR D
80 90 100 110 120 130 140 150 160 170 180
TRAC (NS)


110C
25C
-55C
ACCESS TIME FROM CAS
VCC = 4.50V
VENDOR A
VENDOR B
VENDOR C
VENDOR D
20 30 40 50 60 70 80 90 100 110 120
tCAC (NS)


110C
25C
-55C
RANDOM READ OR WRITE
CYCLE TIME
VCC = 4.50V
VENDOR A
VENDOR B
VENDOR C
VENDOR D
100 120 140 160 180 200 220 240 260
TRC (NS)


110C
25C
-55C
RAS PRECHARGE TIME
VCC = 4.50V
VENDOR A
VENDOR B
VENDOR C
VENDOR D
0 10 20 30 40 50 60 70 80 90 100
TRP (NS)


-55C
25C
110C
RAS/CAS SUPPLY CURRENT
VCC = 5.50V
VENDOR A
VENDOR B
VENDOR C
VENDOR D
20
25
30
35
40
45
50
55
60
ICC (MA)

APPENDIX VIII

OUTPUT DISABLE DELAY

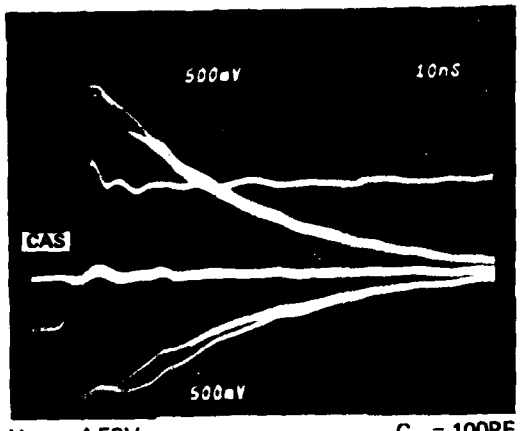
OUTPUT DISABLE DELAY

VENDOR A

500 MV/DIV. VERTICAL
10 NS/DIV. HORIZONTAL

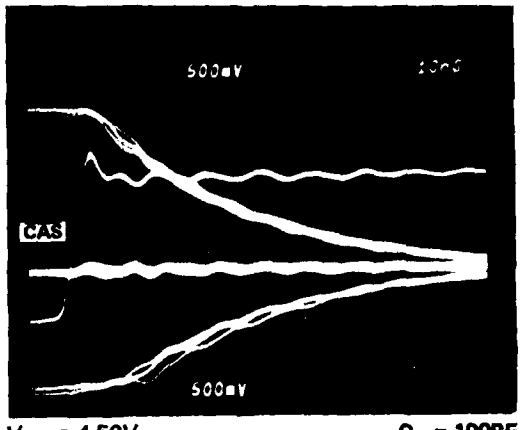
VENDOR B

OUTPUT DISABLE VS. TEMPERATURE (-55, 25, 110°C)



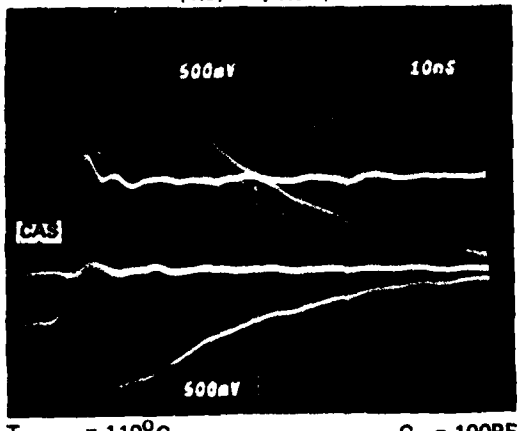
V_{CC} = 4.50V C_L = 100PF

OUTPUT DISABLE VS. TEMPERATURE (-55, 25, 110°C)



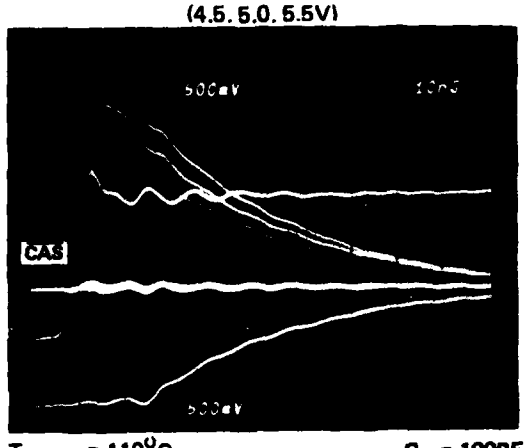
V_{CC} = 4.50V C_L = 100PF

OUTPUT DISABLE VS. SUPPLY VOLTAGE (4.5, 5.0, 5.5V)



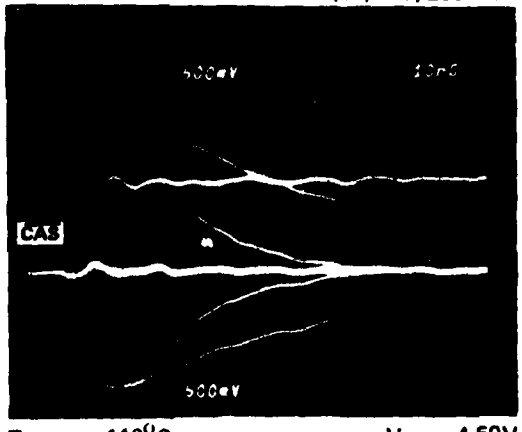
T_{CASE} = 110°C C_L = 100PF

OUTPUT DISABLE VS. SUPPLY VOLTAGE (4.5, 5.0, 5.5V)



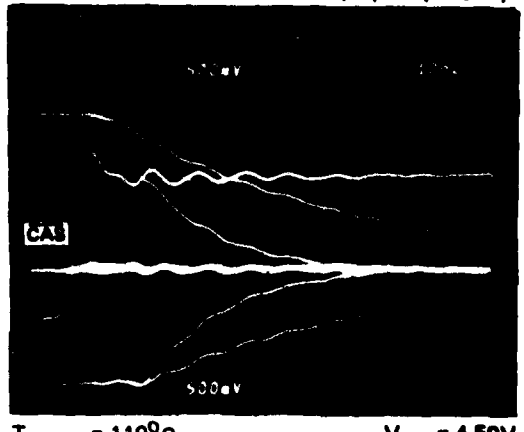
T_{CASE} = 110°C C_L = 100PF

OUTPUT DISABLE VS. LOAD (44, 100, 200PF)



T_{CASE} = 110°C V_{CC} = 4.50V

OUTPUT DISABLE VS. LOAD (44, 100, 200PF)



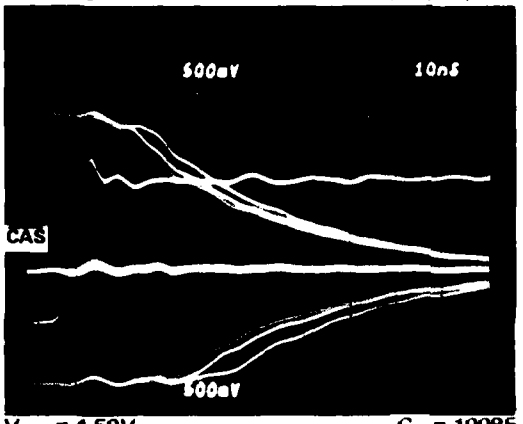
T_{CASE} = 110°C V_{CC} = 4.50V

OUTPUT DISABLE DELAY

500 MV/DIV. VERTICAL
10 NS/DIV. HORIZONTAL

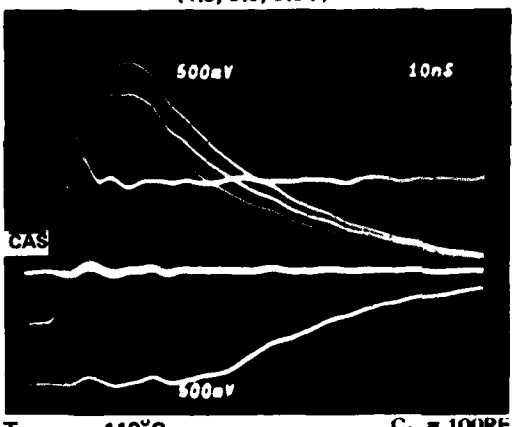
VENDOR C

OUTPUT DISABLE VS. TEMPERATURE (-55, 25, 110°C)



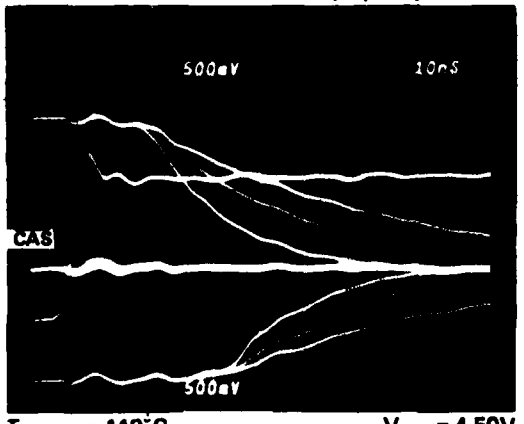
V_{CC} = 4.50V C_L = 100PF

OUTPUT DISABLE VS. SUPPLY VOLTAGE (4.5, 5.0, 5.5V)



T_{CASE} = 110°C C_L = 100PF

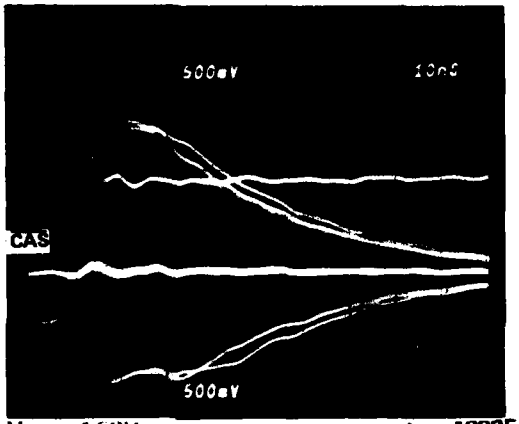
OUTPUT DISABLE VS. LOAD (44, 100, 200 PF)



T_{CASE} = 110°C V_{CC} = 4.50V

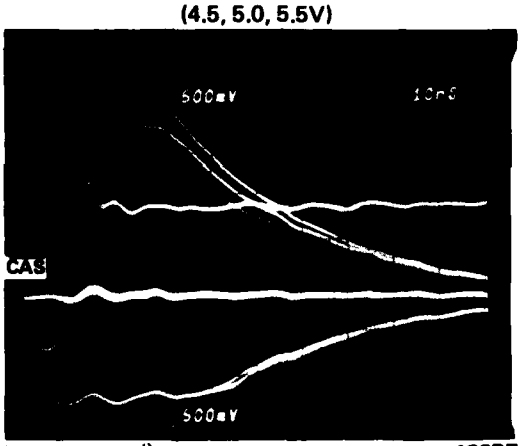
VENDOR D

OUTPUT DISABLE VS. TEMPERATURE (-55, 25, 110°C)



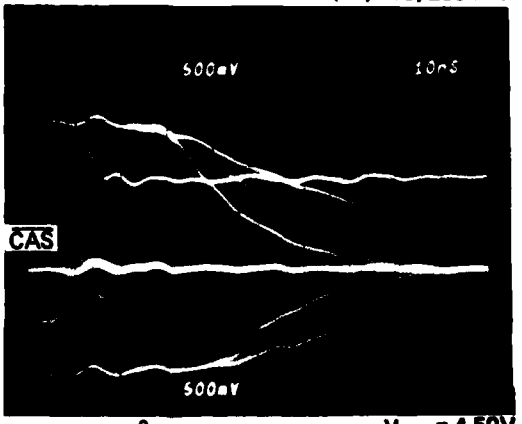
V_{CC} = 4.50V C_L = 100PF

OUTPUT DISABLE VS. SUPPLY VOLTAGE (4.5, 5.0, 5.5V)



T_{CASE} = 110°C C_L = 100PF

OUTPUT DISABLE VS. LOAD (44, 100, 200 PF)



T_{CASE} = 110°C V_{CC} = 4.50V

APPENDIX IX

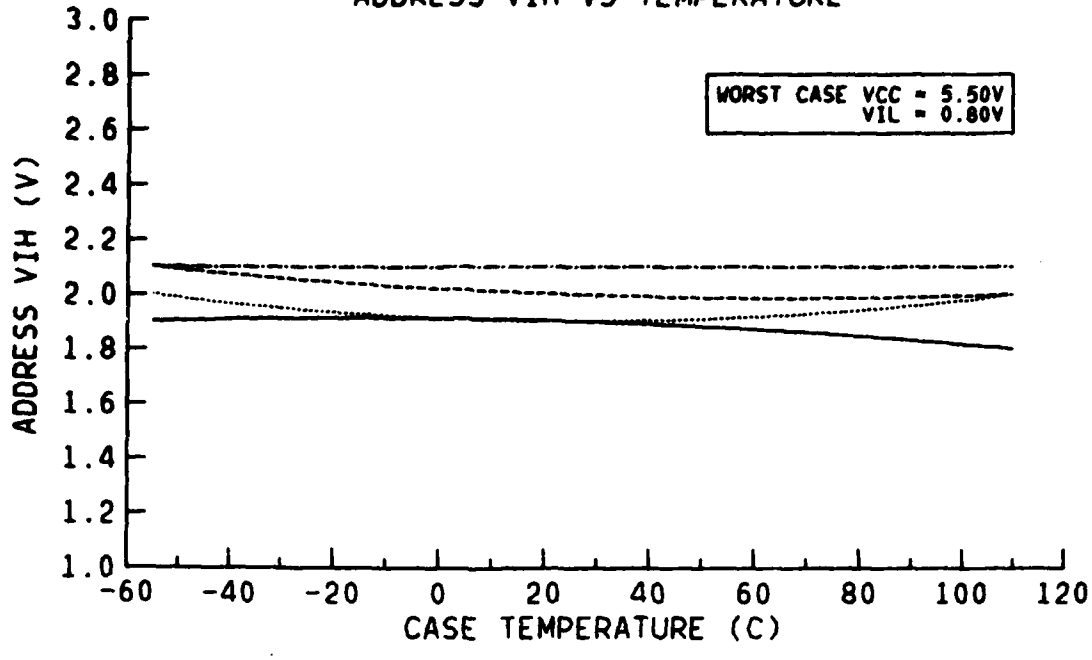
INPUT LEVEL SENSITIVITY

VENDOR A
VENDOR B
VENDOR C
VENDOR D

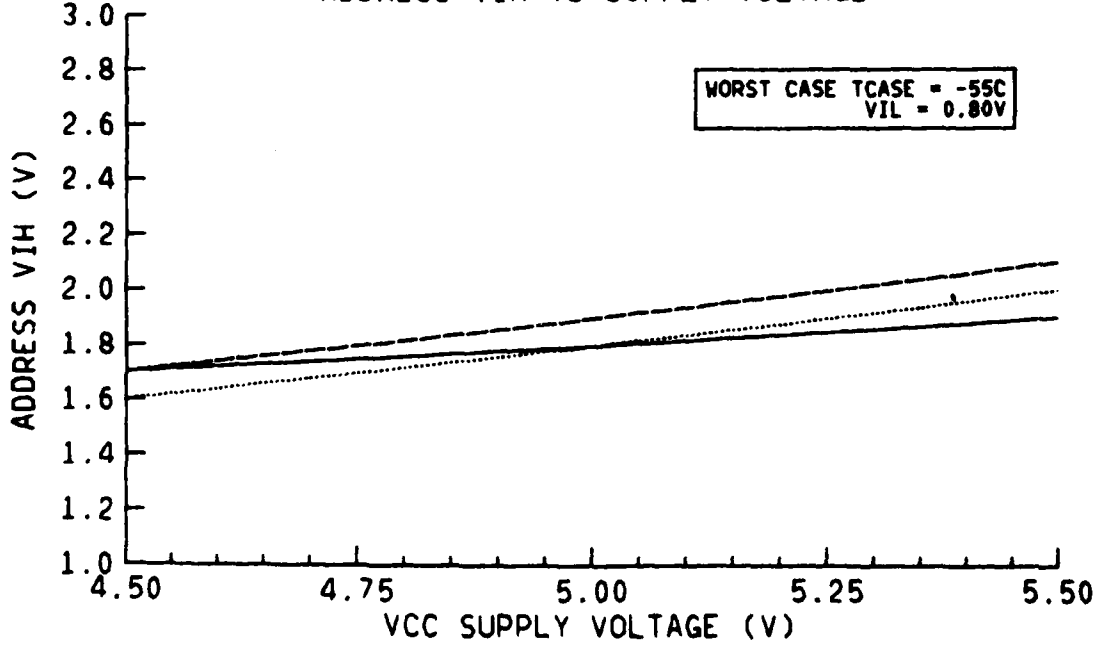
ADDRESS INPUT HIGH LEVEL

PROPOSED LIMIT
2.40V MIN

ADDRESS VIH VS TEMPERATURE



ADDRESS VIH VS SUPPLY VOLTAGE

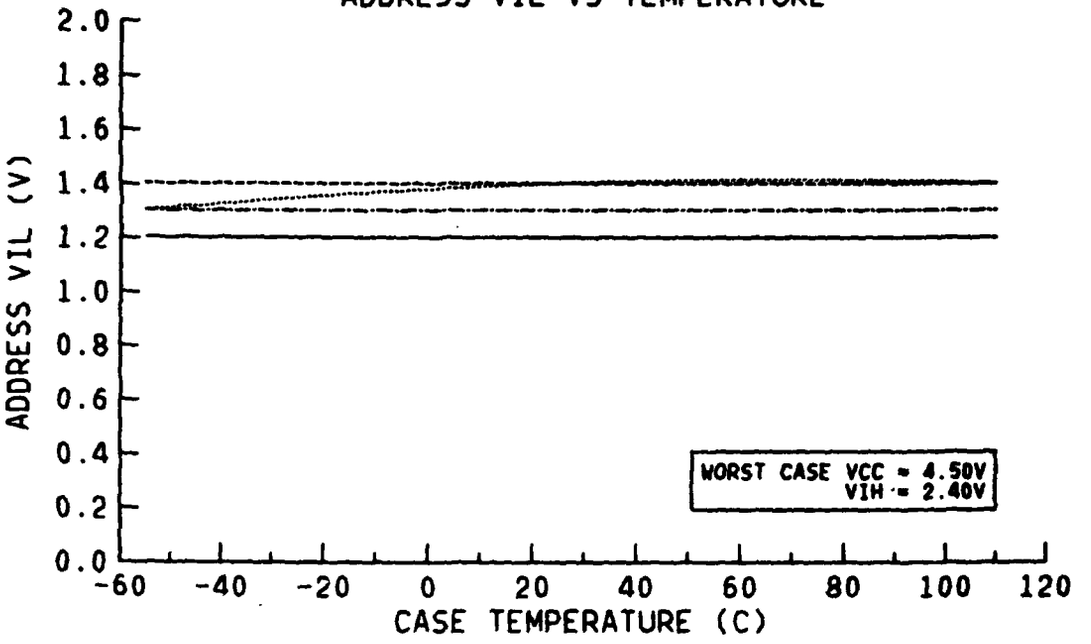


VENDOR A
VENDOR B
VENDOR C
VENDOR D

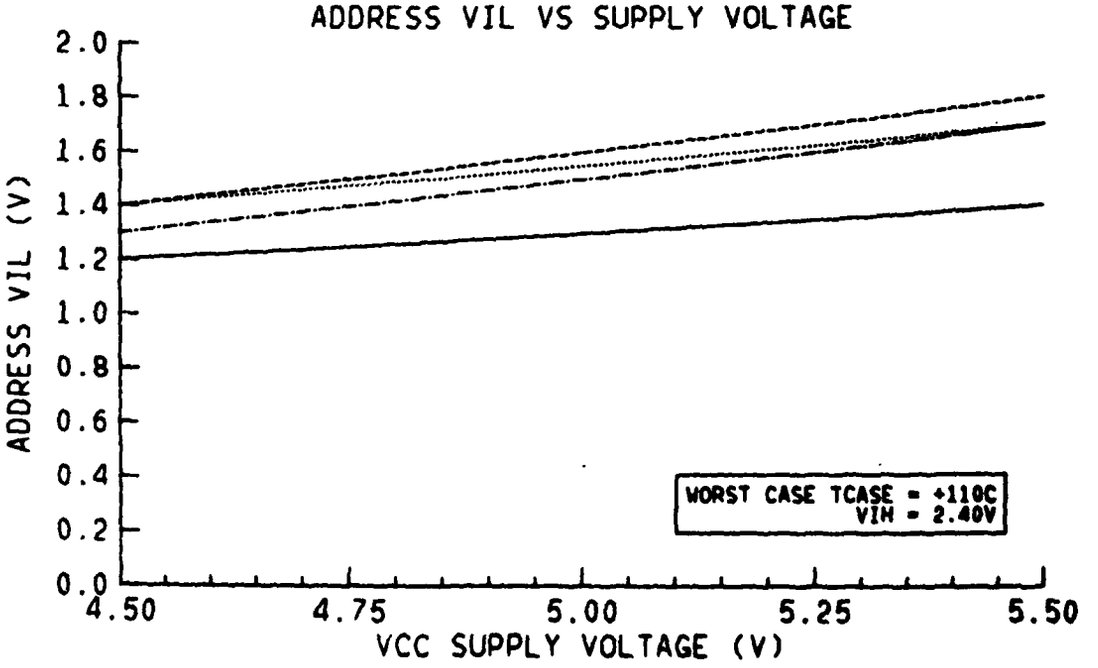
ADDRESS INPUT LOW LEVEL

PROPOSED LIMIT
0.80V MAX

ADDRESS VIL VS TEMPERATURE



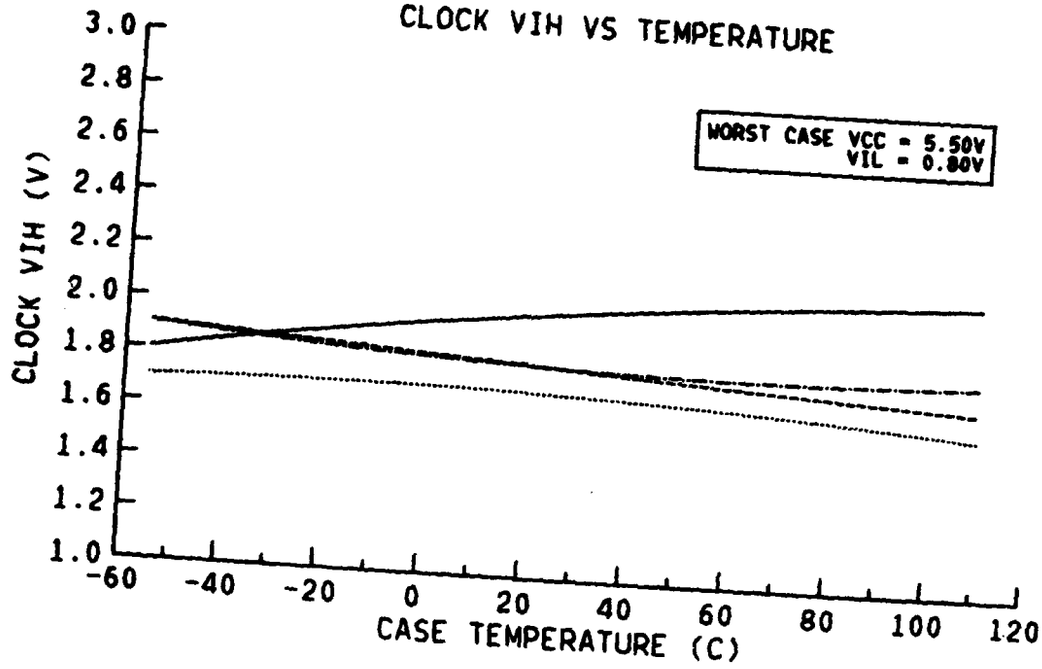
ADDRESS VIL VS SUPPLY VOLTAGE

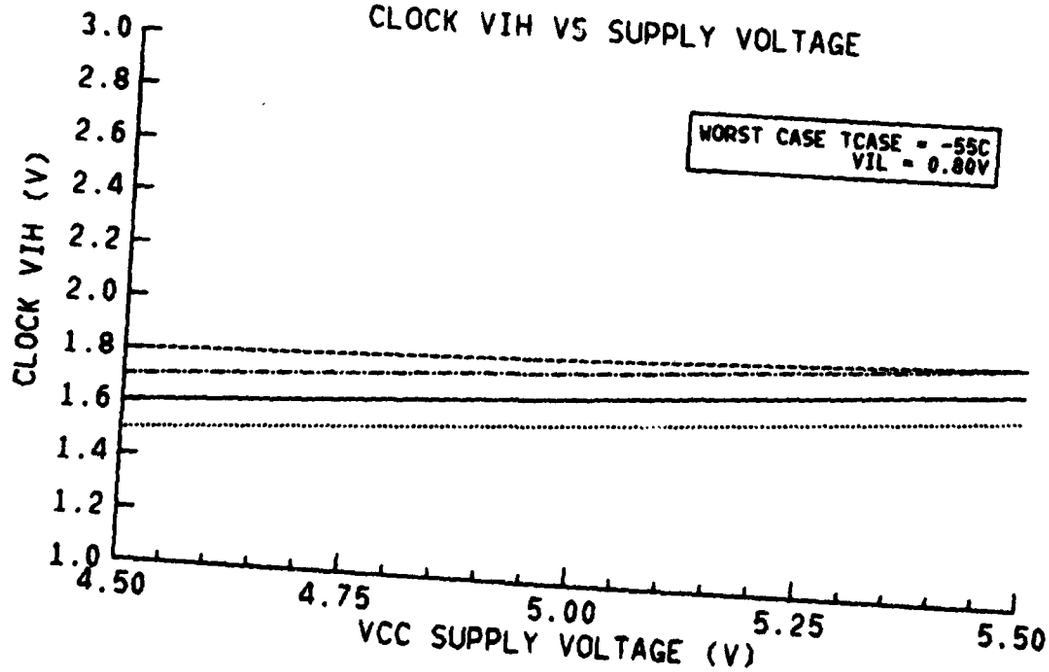


VENDOR A
VENDOR B
VENDOR C
VENDOR D

CLOCK INPUT HIGH LEVEL

PROPOSED LIMIT
2.40V MIN



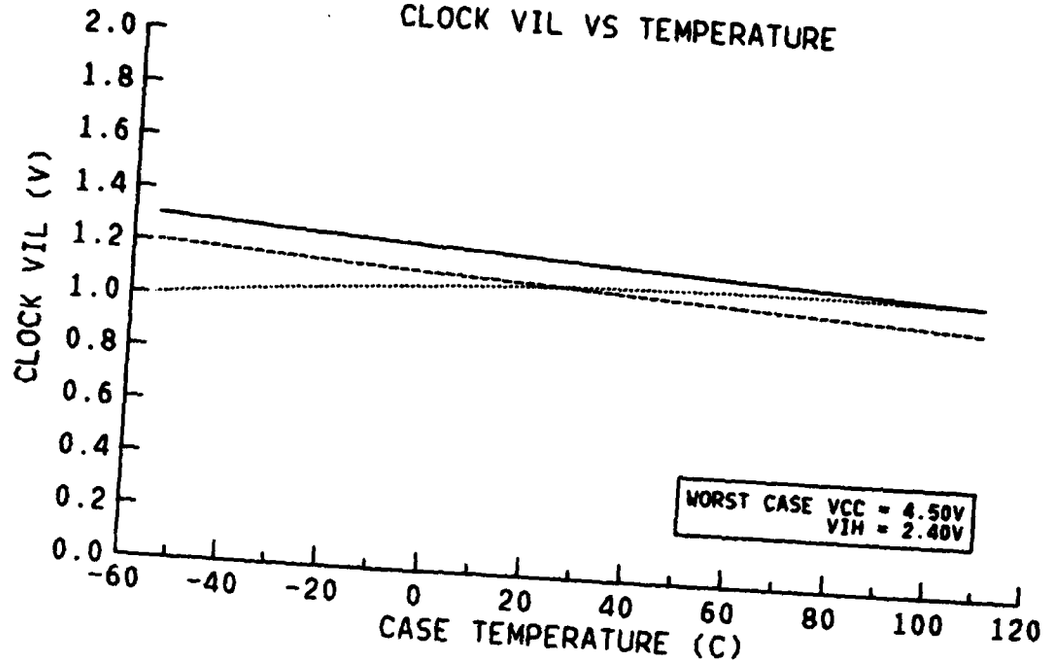


VENDOR A
VENDOR B
VENDOR C
VENDOR D

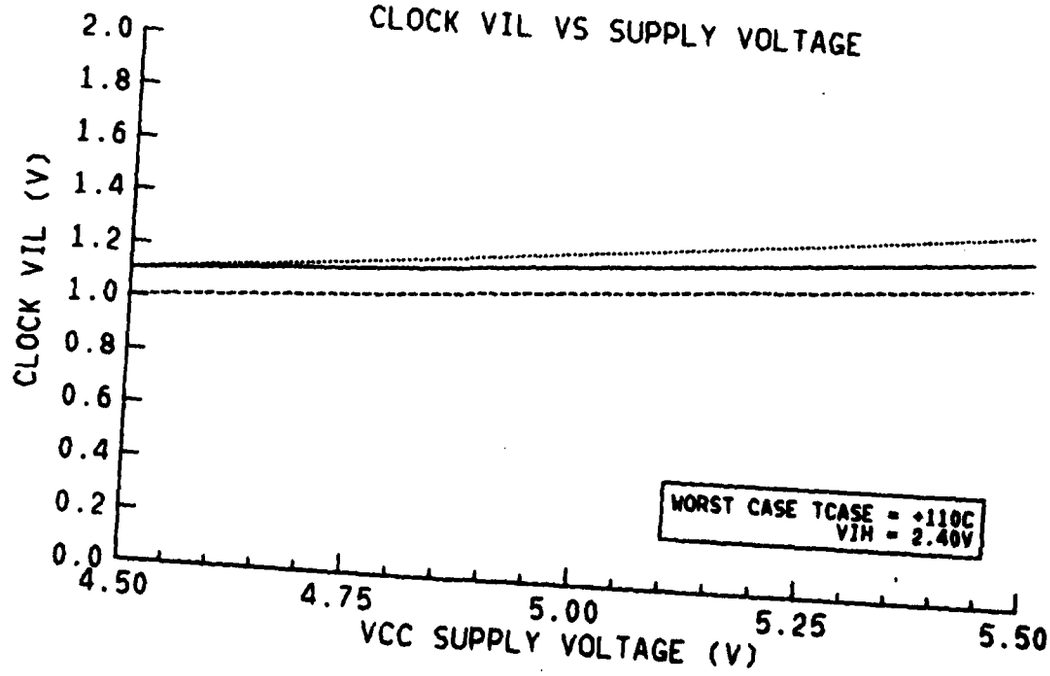
CLOCK INPUT LOW LEVEL

PROPOSED LIMIT
0.80V MAX

CLOCK VIL VS TEMPERATURE



CLOCK VIL VS SUPPLY VOLTAGE



APPENDIX X

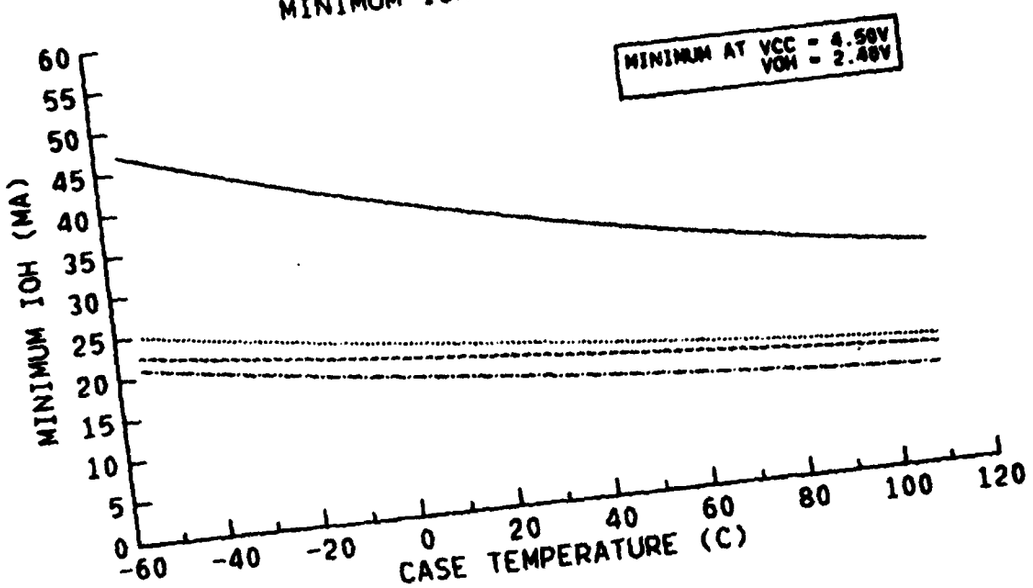
OUTPUT DRIVE CHARACTERISTICS

OUTPUT SOURCE CURRENT

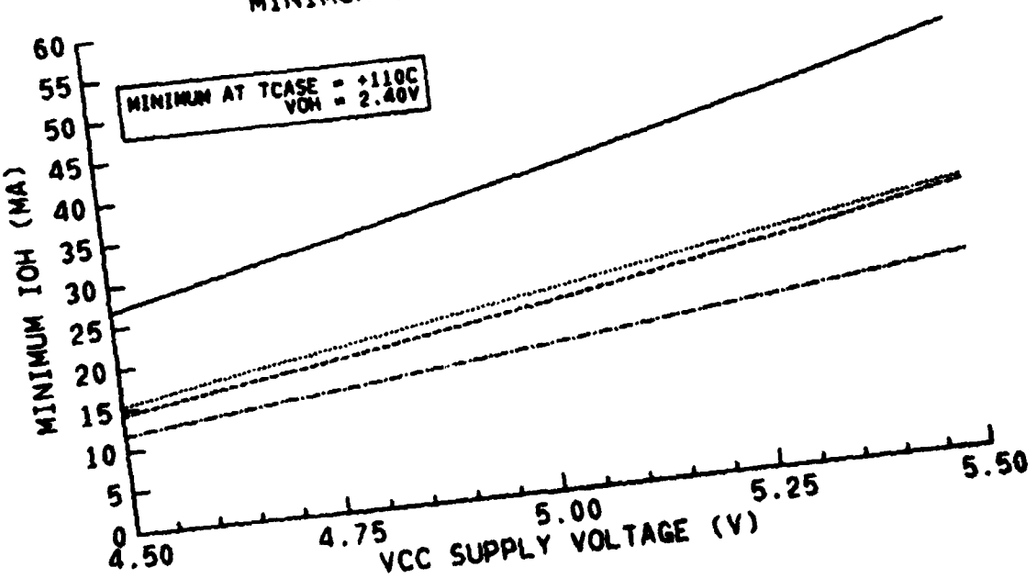
PROPOSED LIMIT
5.0MA MIN

VENDOR A ——
VENDOR B ·····
VENDOR C – – –
VENDOR D —·—·—

MINIMUM IOH VS TEMPERATURE



MINIMUM IOH VS SUPPLY VOLTAGE

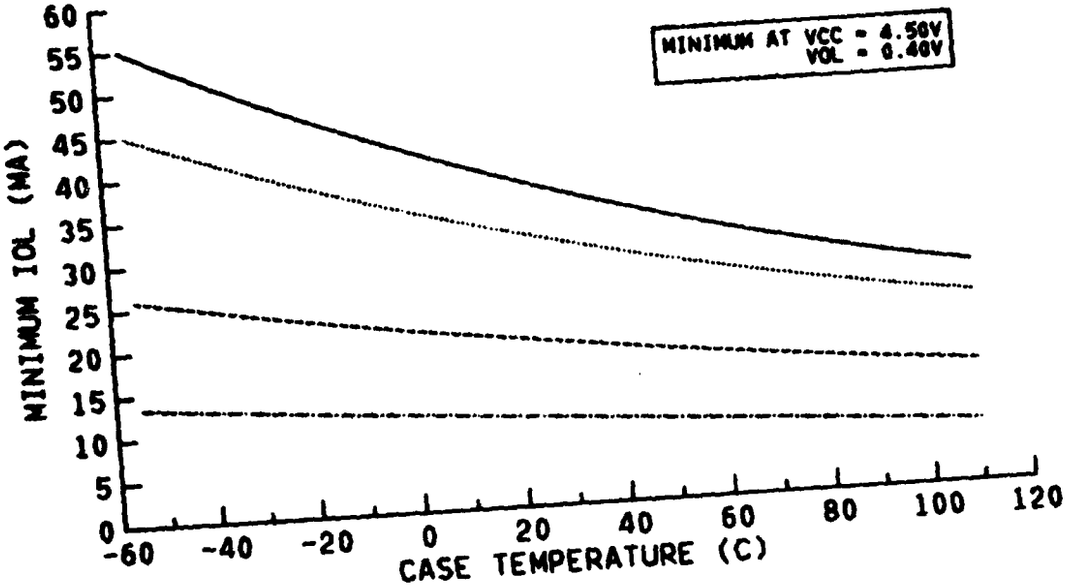


OUTPUT SINK CURRENT

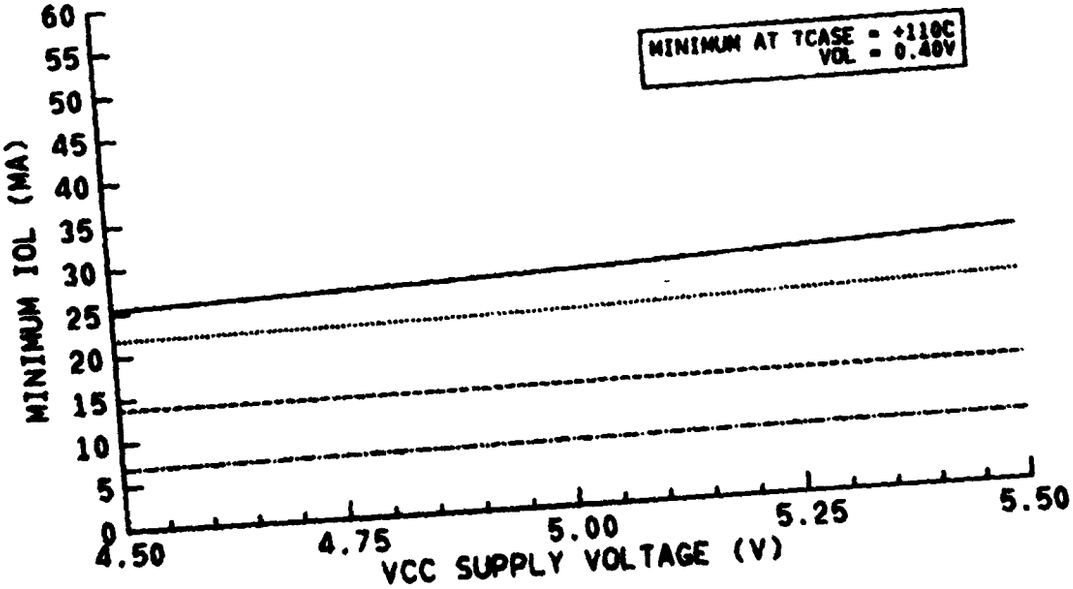
PROPOSED LIMIT
4.0MA MIN

VENDOR A
VENDOR B
VENDOR C
VENDOR D

MINIMUM IOL VS TEMPERATURE



MINIMUM IOL VS SUPPLY VOLTAGE

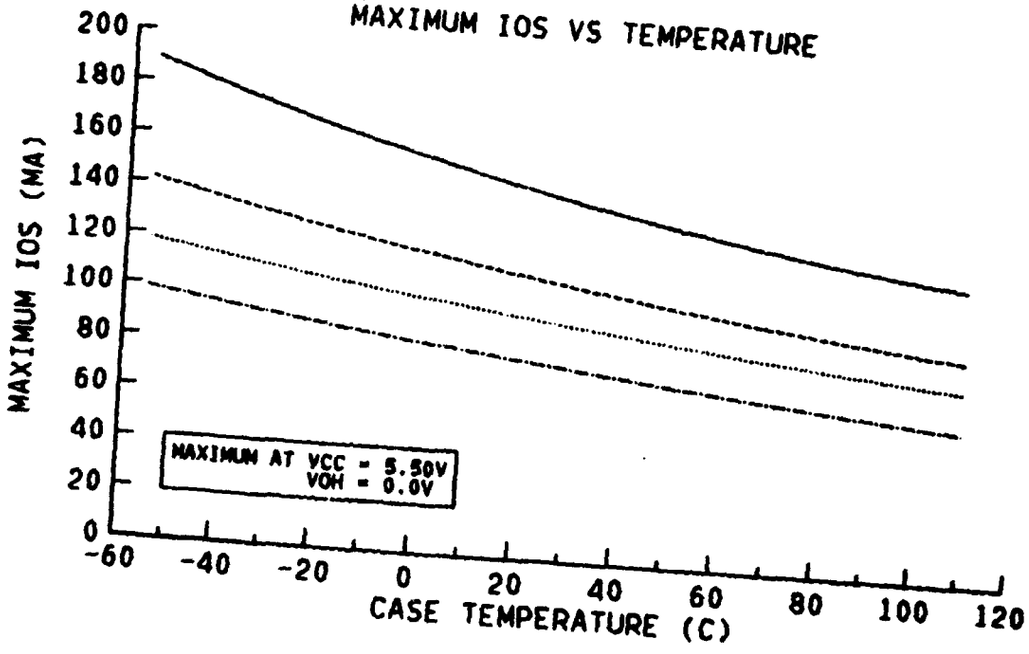


VENDOR A
VENDOR B
VENDOR C
VENDOR D

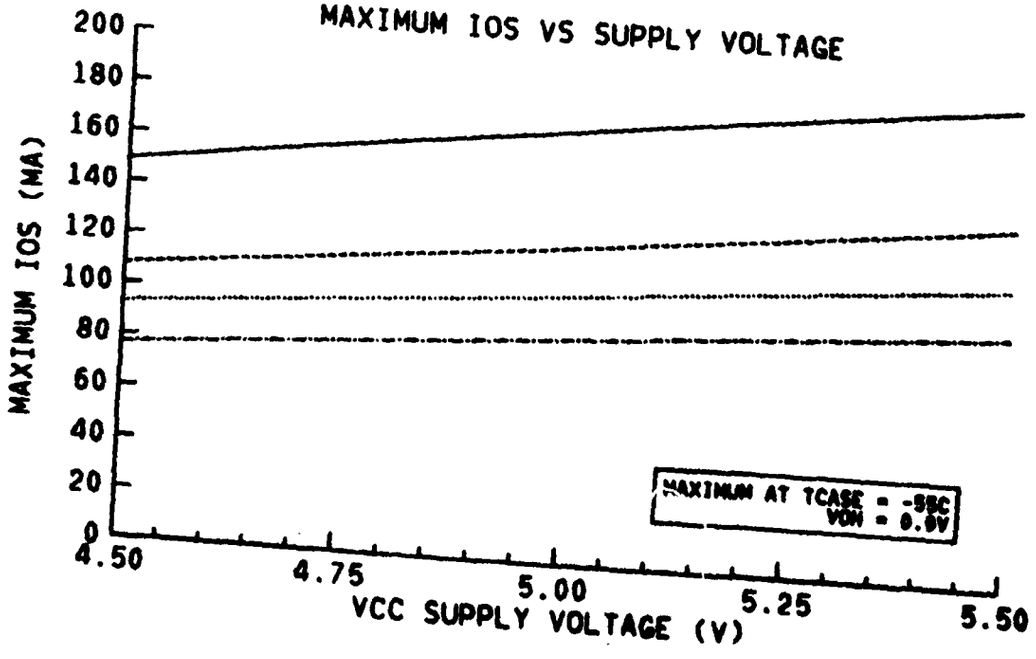
OUTPUT SHORT CIRCUIT CURRENT

PROPOSED LIMIT
150MA MAX

MAXIMUM IOS VS TEMPERATURE



MAXIMUM IOS VS SUPPLY VOLTAGE



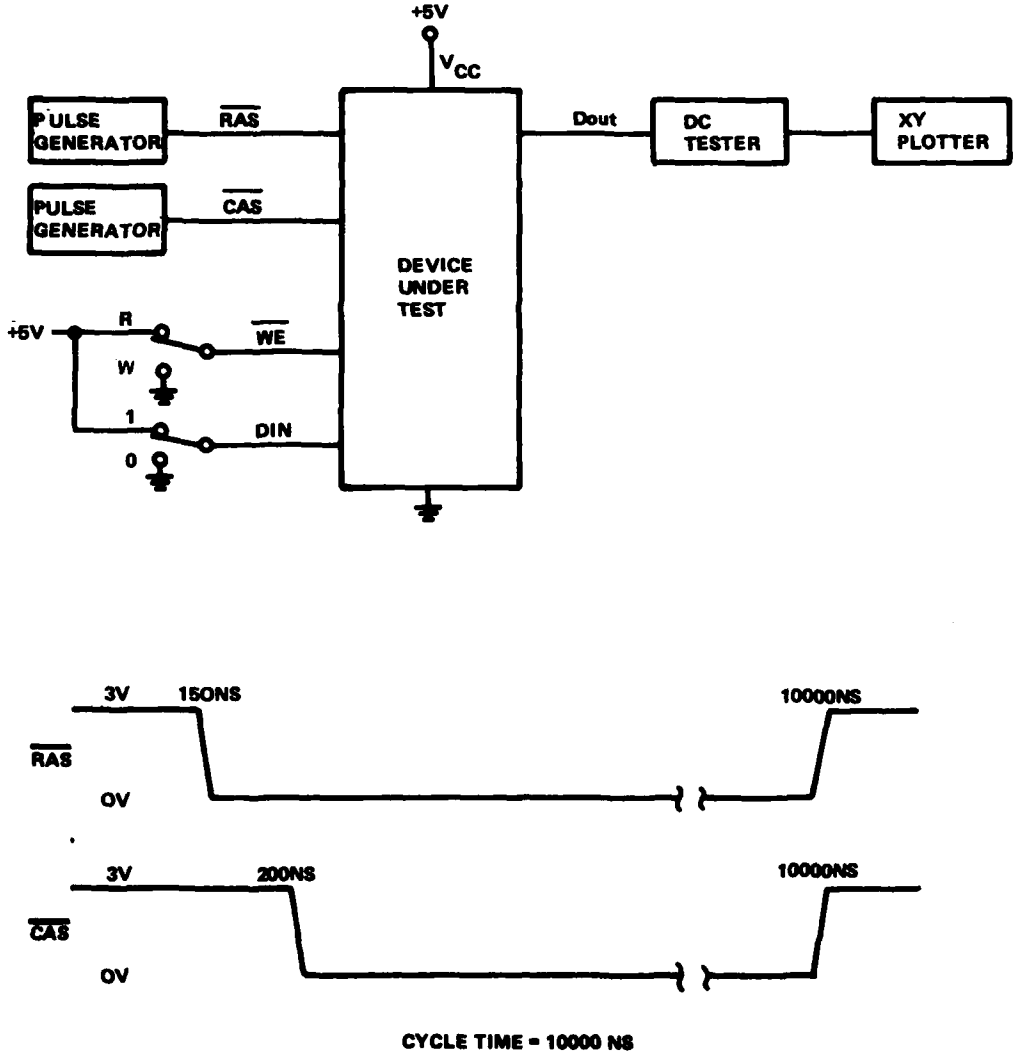
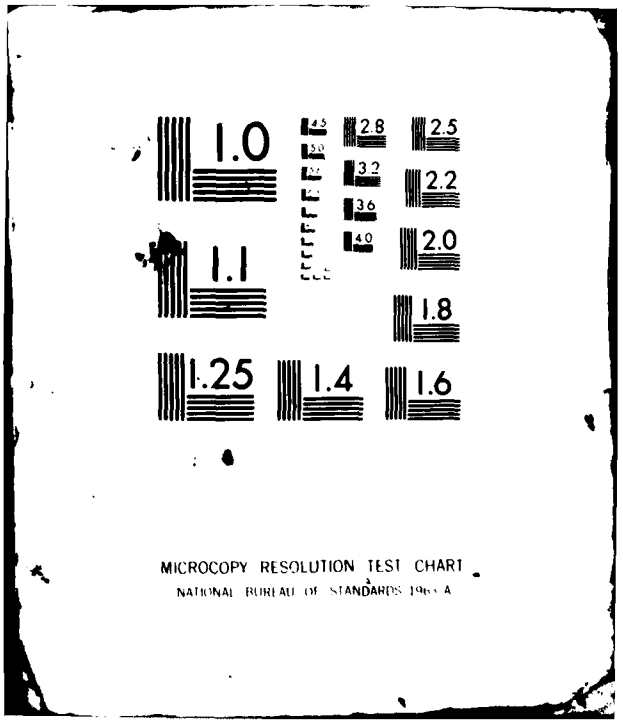


Figure 3. Output Drive Current Test Circuit and Timing

AD-A113 190 IBM FEDERAL SYSTEMS DIV MANASSAS VA F/G 9/2
ELECTRICAL CHARACTERIZATION OF 64K DYNAMIC RAMS.(U)
JAN 82 G MANZO, P PFEIFFER, T COWELL F30602-80-C-0045
UNCLASSIFIED RADC-TR-81-373 NL

2.2

END
DATE FILMED
4 82
DTIC


1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

APPENDIX XI

DEVICE CAPACITANCE

TABLE 4. 64K DYNAMIC RAM DEVICE CAPACITANCE (pF)

	VENDOR			
PIN DESIGNATION	A	B	C	D
AO	3.2	2.7	4.5	4.3
A1	2.6	2.1	2.9	2.8
A2	2.8	2.2	3.6	3.6
A3	3.1	2.5	3.5	3.9
A4	2.9	2.3	3.6	3.6
A5	2.8	2.2	3.4	3.0
A6	4.7	3.3	4.6	4.1
A7	2.3	1.9	2.9	2.5
$\overline{RAS}$	3.7	3.1	3.1	4.8
$\overline{CAS}$	4.4	3.4	6.2	3.5
$\overline{WE}$	2.7	3.5	3.3	4.4
D_{IN}	2.6	2.3	3.3	3.2
D_{OUT}	4.1	5.0	5.4	4.7

APPENDIX XII

FUNCTIONAL ALGORITHMS, TIMING SETS, AND TIMING WAVEFORMS

Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion.

Timing sets are displayed in Table 5. Note that multiple passes through the memory are required to screen MIL-M-38510/244. The timing conditions and input levels shown in Table 5 are recommended and will properly screen MIL-M-38510/244 limits. Equivalent timing sets may be used that serve the same purpose.

NOTE: Step 1 of all algorithms may be performed initially and if testing is continuous (no dead time exceeding 5 ms between tests), step 1 does not have to be repeated for each algorithm.

PATTERN 1

CONTINUOUS READ, DATA BACKGROUND = X-BAR

This pattern is used to allow the maximum amount of current I_{CC} to be drawn from the V_{CC} power supply. It is performed in the following manner with normal cycle timing:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Sequentially read entire memory
Step 4 - Repeat step 3 as many times as necessary to achieve a reading

Test time - Undefined

PATTERN 2

OUTPUT HIGH IMPEDANCE (t_{off})

This pattern verifies the output buffer switches to high impedance (tri-state) within the specified 35NS after the rise of $\overline{CAS}$. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load minimum address location with "0"
Step 3 - Read minimum address location and measure V_{OL}
Step 4 - Raise $\overline{CAS}$ and measure $V_{OUT} \leq V_{OL}$ + 0.5V after 35NS delay
Step 5 - Load minimum address location with "1"
Step 6 - Read minimum address location and measure V_{OH}
Step 7 - Raise $\overline{CAS}$ and measure $V_{OUT} \geq V_{OH}$ -0.5V after 35NS delay

Test time = 12 x cycle time

PATTERN 3

V_{BUMP}/V_{BOBBLE}, DATA BACKGROUND = ALL "0" (Discharged State)

This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Pause 40µs ramping V_{CC} to 4.5v inhibiting all clocks
Step 3 - Load memory with background data
Step 4 - Pause 40µs ramping V_{CC} to 5.5v inhibiting all clocks
Step 5 - Read memory with background data
Step 6 - Repeat Steps 2 through 5 for background data complement
Step 7 - Load memory with background data
Step 8 - Pause 40µs ramping V_{CC} to 4.5v inhibiting all clocks
Step 9 - Read memory with background data
Step 10- Pause 40µs ramping V_{CC} to 5.5v inhibiting all clocks
Step 11- Repeat steps 7 through 9 for background data complement

Test time = (8N + 8) x cycle time + 280µs

PATTERN 4

ADDRESS COMPLEMENT, DATA BACKGROUND = ALL "0"

This pattern produces maximum address line noise and checks the decoder dynamic response times. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read minimum address location
Step 4 - Load minimum address location with "1"
Step 5 - Read maximum address location
Step 6 - Load maximum address location with "1"
Step 7 - Read minimum address location + 1
Step 8 - Load minimum address location +1 with "1"
Step 9 - Read maximum address location -1
Step 10 - Load maximum address location -1 with "1"
Step 11 - Repeat steps 3 through 10 until all address locations have been read and loaded with "1"s.
Step 12 - Repeat steps 3 through 11 reading "1"s and loading "0"s.

Test time = (5N + 8) x cycle time

PATTERN 5

SHIFTING DIAGONAL, INITIAL DATA BACKGROUND = MAJOR DIAGONAL

This pattern is a good test for sense line imbalance and response plus restore noise in addition to multiple selection. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with data background, scan from minimum location to maximum location
Step 3 - Read data in the memory, scan from maximum location to minimum location
Step 4 - Repeat steps 2 and 3, each time shifting the diagonal by one until it has occupied every position in the memory (256 load/read scans)
Step 5 - Repeat steps 2 through 4 with complement data

Test time = (512N + 8) x cycle time

PATTERN 6

MARCH DATA, DATA BACKGROUND = ALL "0"

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data

Step 3 - Read location 0
Step 4 - Write data complement in location 0
Step 5 - Read data complement in location 0
Step 6 - Repeat steps 3 through 5 for all other locations in memory (sequentially)
Step 7 - Read data complement at maximum location
Step 8 - Write data at minimum location
Step 9 - Read data at minimum location
Step 10 - Repeat steps 7 through 9 for all other locations in the memory (sequentially)
Step 11 - Repeat steps 2 through 10 with data background of all "1"

Test time = (14N + 8) x cycle time

PATTERN 7

STATIC REFRESH (PERIPHERY RETENTION)

This pattern tests for periphery retention time by attempting to write after a lengthy pause. This test is performed at 110°C (case) only, and is not used to measure the retention time of the periphery circuits, but to insure that they will hold for at least 5 ms. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with all "0"s
Step 3 - Read memory, all "0"s
Step 4 - Pause (stop all clocks) 5 ms
Step 5 - Load memory with all "1"s
Step 6 - Read memory, all "1"s
Step 7 - Pause (stop all clocks) 5 ms
Step 8 - Load memory with all "0"s
Step 9 - Read memory, all "0"s

Test time = (6N + 8) x cycle time + 10 ms

PATTERN 8

REFRESH TEST (CELL RETENTION)

This test is used to check the retention time of memory cells under static and dynamic conditions. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with all "0"s
Step 3 - Pause 1 ms (stop all clocks)
Step 4 - Read memory, all "0"s
Step 5 - Repeat steps 2 through 4 will all "1"s
Step 6 - Read minimum address location

Step 7 - Read maximum address location
Step 8 - Repeat Step 6 and 7 for 1 ms
Step 9 - Read memory, all "1"s
Step 10 - Load memory, all "0"s
Step 11 - Repeat steps 6 through 9 with all "0"s
Step 12 - Read address location 32767
Step 13 - Read address location 32768
Step 14 - Repeat steps 12 and 13 for 1 ms
Step 15 - Read memory, all "0"s
Step 16 - Load memory, all "1"s
Step 17 - Repeat steps 12 through 15 with all "0"s

Test time = (10N + 8) x cycle time + 6 ms

PATTERN 9

EXTENDED CYCLE TEST (10μs), DATA BACKGROUND = X-BAR

This test is used to verify the 10μs maximum limit on RAS and CAS pulse widths. Front and back edge timing is held to normal cycle timing while the cycle is increased to allow 10μs of $\overline{RAS}$ and $\overline{CAS}$ active time (low level). It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Write data in location 0
Step 3 - Read data in location 0
Step 4 - Repeat steps 2 and 3 for all other locations in the memory (sequentially)
Step 5 - Repeat steps 2 through 4 with complement data

Test time = (4N + 8) x cycle time

PATTERN 10

RAS-ONLY/REFRESH TEST

This test is used to verify the functionality of the $\overline{RAS}$-only mode of cell refreshing. It is done at high temperature only and is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with all "0"s
Step 3 - Perform 128 RAS-only cycles ($\overline{CAS} \neq \overline{WE}$ = "1")
Step 4 - Repeat step 3 for 10 seconds
Step 5 - Read memory, all "0"s
Step 6 - Repeat step 2 through 5 with all "1"s

Test time = (4N + 8) x cycle time + 20 seconds

PATTERN 11

READ-MODIFY-WRITE (RMW), DATA BACKGROUND = ALL "0"

This pattern verifies the Read-Modify-Write mode for the memory. It is performed in the following manner:

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read minimum address location and load with "1" using RMW cycle
Step 4 - Read maximum address location and load with "1" using RMW cycle
Step 5 - Read minimum address location +1 and load with "1" using RMW cycle
Step 6 - Read maximum address location -1 and load with "1" using RMW cycle
Step 7 - Repeat steps 3 through 6 until all address locations have been read and loaded with "1"
Step 8 - Repeat steps 3 through 7 reading "1"s and loading "0"s
Step 9 - Read memory, all "0"s

Test time = (2N + 8) x read or write cycle time + (2N) x read-modify-write cycle time

TABLE 5. RECOMMENDED TIMING SET DESIGNATION FOR SCREENING MIL-M-38510/244 LIMITS

PARAMETER NUMBER	SYMBOL	SPEC LIMIT (NS)	TS#1	TS#2	TS#3	TS#4 (NOMINAL)	TS#5 (RMW)	TS#6 (EXTENDED)
1a	t_{RC} MIN	250	250*	250*	310	320	-	-
b	MAX	10100	-	-	-	-	-	10100*
2a	t_{RMW} MIN	270	-	-	-	-	270*	-
b	MAX	10100	-	-	-	-	-	-
3	t_{RAC} MAX	150	150*	150*	210	150*	-	150*
4	t_{CAC} MAX	90	-	90*	90*	95	90*	-
5	t_{RP} MIN	90	90*	90*	90*	120	100	90*
6a	t_{RAS} MIN	150	150*	150*	210	180	160	-
b	MAX	10000	-	-	-	-	-	10000*
7	t_{RSH} MIN	90	130	90*	90*	125	100	9975
8	t_{CSH} MIN	150	240	150*	210	280	160	10025
9a	t_{CAS} MIN	90	220	90*	125	225	100	-
b	MAX	10000	-	-	-	-	-	10000*
10a	t_{RCD} MIN	25	25*	-	-	-	-	25*
b	MAX	60	-	60*	115	55	60*	-
11	t_{ASR} MIN	0	0*	0*	0*	10	0*	0*
12	t_{RAH} MIN	20	20*	55	120	30	55	20*
13	t_{ASC} MIN	-5	-5*	-5*	-5*	5	-5*	-5*
14	t_{CAH} MIN	30	55	30*	30*	75	30*	55
15	t_{AR} MIN	80	80*	90	150	130	90	80*
16	t_{RCS} MIN	0	0*	0*	0*	-	-	0*
17	t_{RCH} MIN	0	0*	25	0*	-	-	0*
18	t_{WCH} MIN	45	95	90	45*	85	NA	95
19	t_{WCR} MIN	120	120*	150	165	140	160	120*
20	t_{WP} MIN	45	100	45*	50	100	45*	100
21	t_{RWL} MIN	45	130	45*	95	125	45*	9980
22	t_{CWL} MIN	45	220	45*	125	240	45*	10005
23a	t_{DS}(CAS) MIN	0	0*	-	0*	10	-	0*
b	t_{DS}(WE) MIN	0	-	0*	-	-	0*	-
24a	t_{DH}(CAS) MIN	45	95	-	45*	85	-	95
b	t_{DH}(WE) MIN	45	-	45*	-	-	45*	-
25	t_{DHR} MIN	120	120*	140	165	140	160	120*
26	t_{WCS} MIN	0	0**	-40	0**	10	NA	0*
27	t_{CRP} MIN	0	0*	90	60	20	100	65
28	t_{RRH} MIN	25	90	25*	30	-	-	25*
29	t_{CWD} MIN	50	NA	NA	NA	NA	50*	NA
30	t_{RWD} MIN	110	NA	NA	NA	NA	110*	NA

NOTES: * INDICATES PARAMETER BEING TESTED AT SPEC LIMIT
NA - NOT APPLICABLE
TS#1, #2, #3, #5, #6 - USE $V_{IH\ MIN}$ (2.4v) AND $V_{IL\ MAX}$ (0.8v) AND $t_{TRANSISTION}$ = 5nS

TS#4 - NOMINAL TIMING; WILL NOT VIOLATE LIMITS IF $V_{IH\ MAX}$ (6.5v) AND $V_{IL\ MIN}$ (-1.5v) AND $t_{TRANSISTION}$ = 10nS ARE USED

** WHEN SCREENING TWCS, DATA OUT (PIN #14) MUST BE CHECKED FOR A HI-IMPEDANCE STATE DURING A WRITE CYCLE VIA LEAKEAGE TEST METHOD.

READ CYCLE TIMING

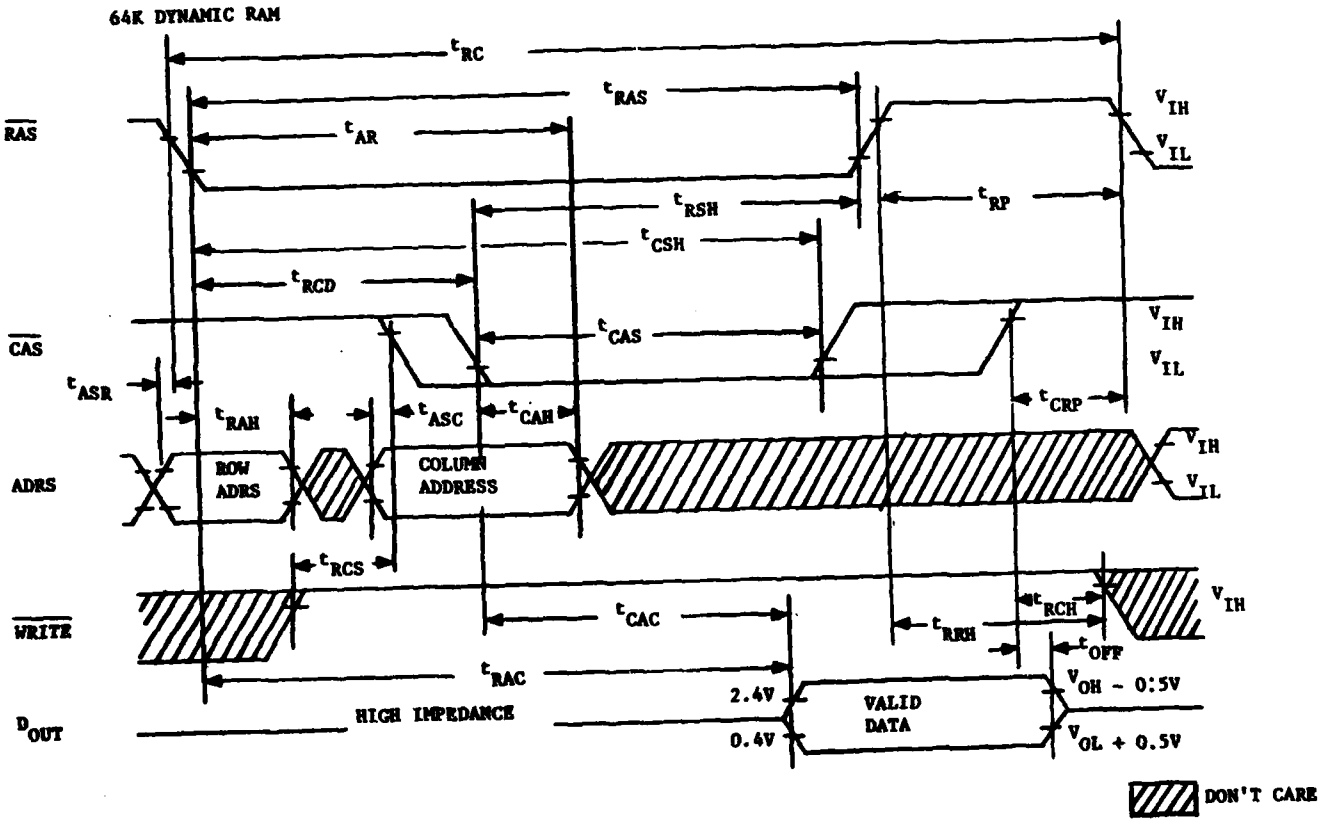


FIGURE 4. READ CYCLE WAVEFORMS

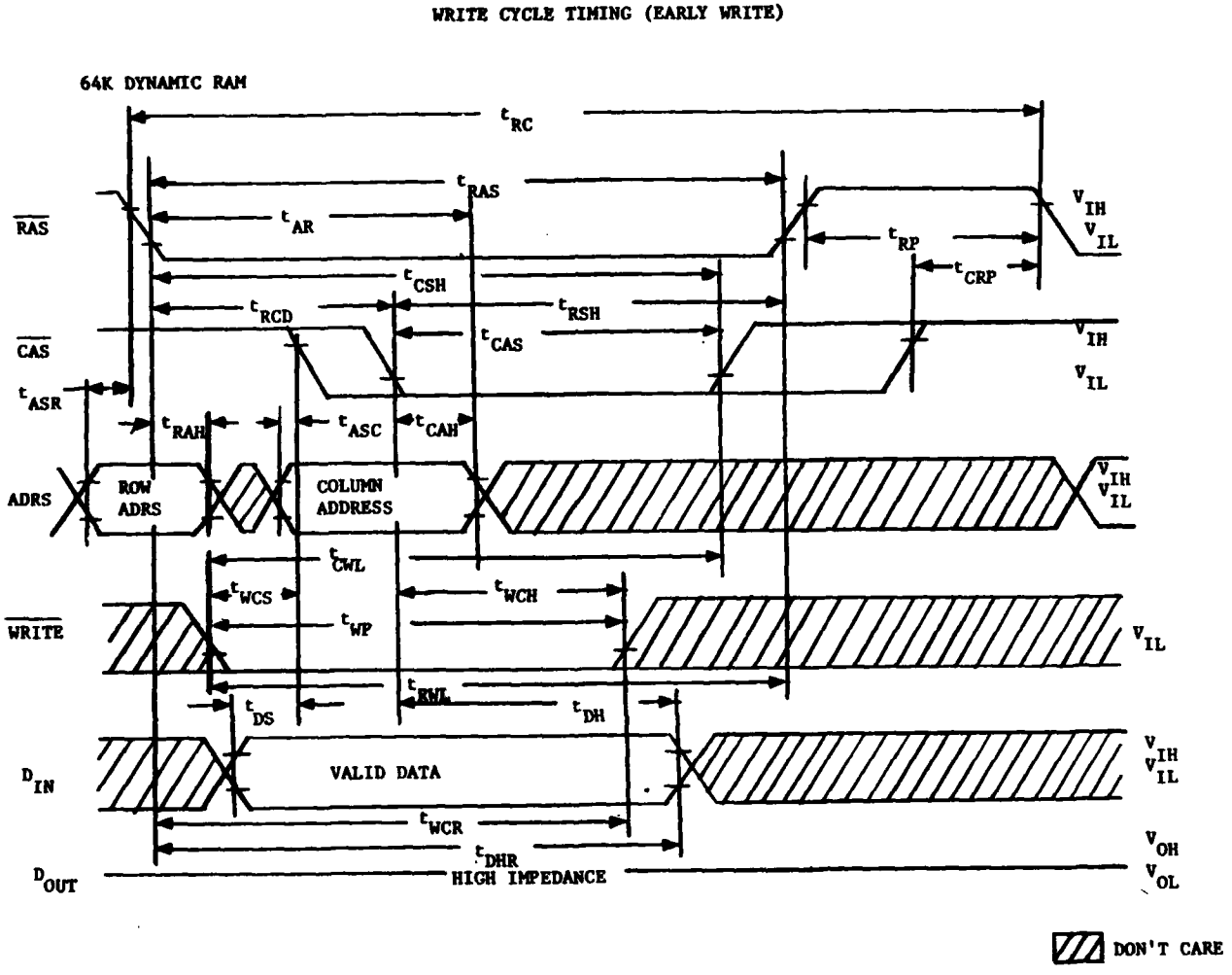


FIGURE 5. WRITE CYCLE WAVEFORMS

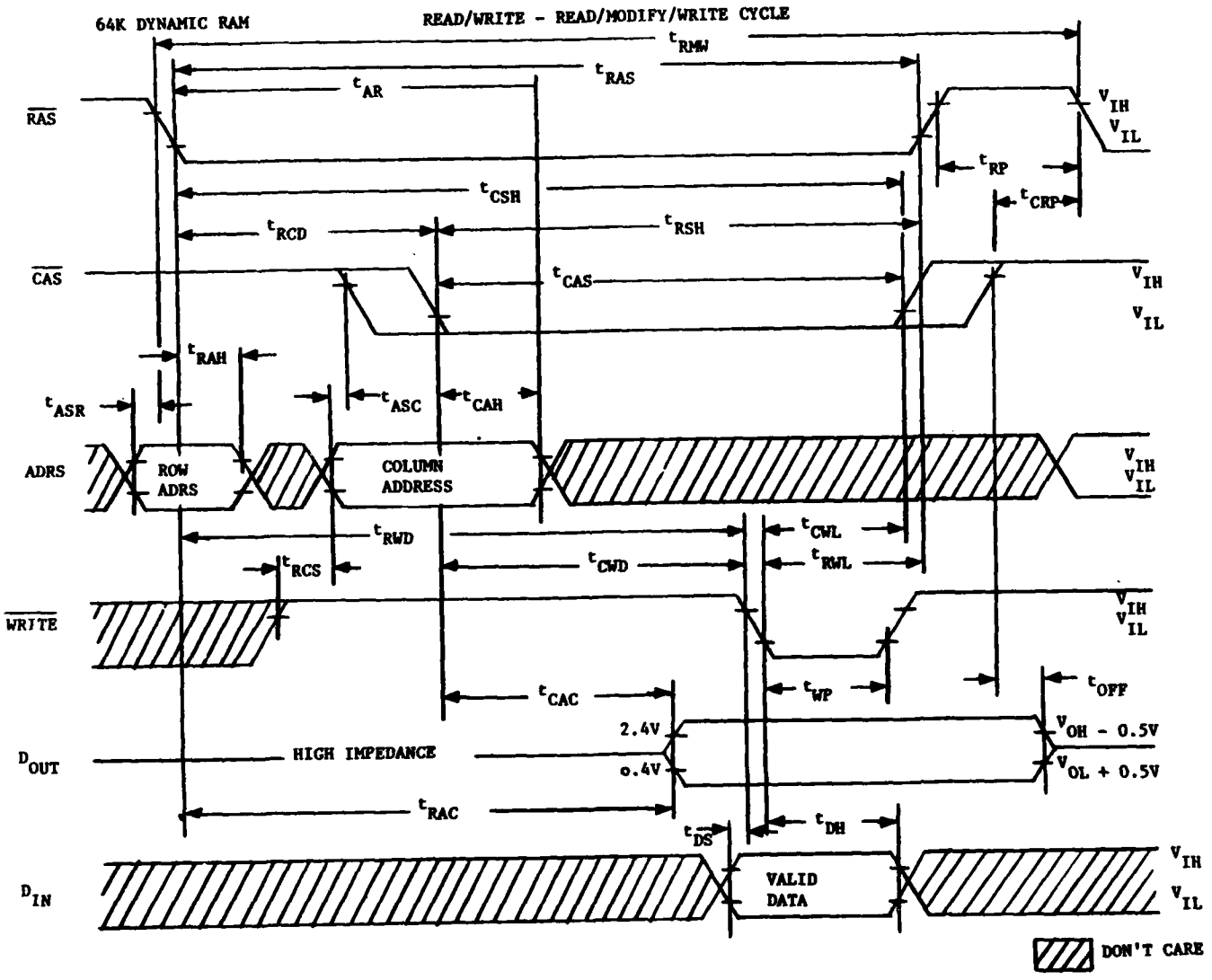


FIGURE 6. READ/WRITE, READ/MODIFY/WRITE CYCLE WAVEFORMS

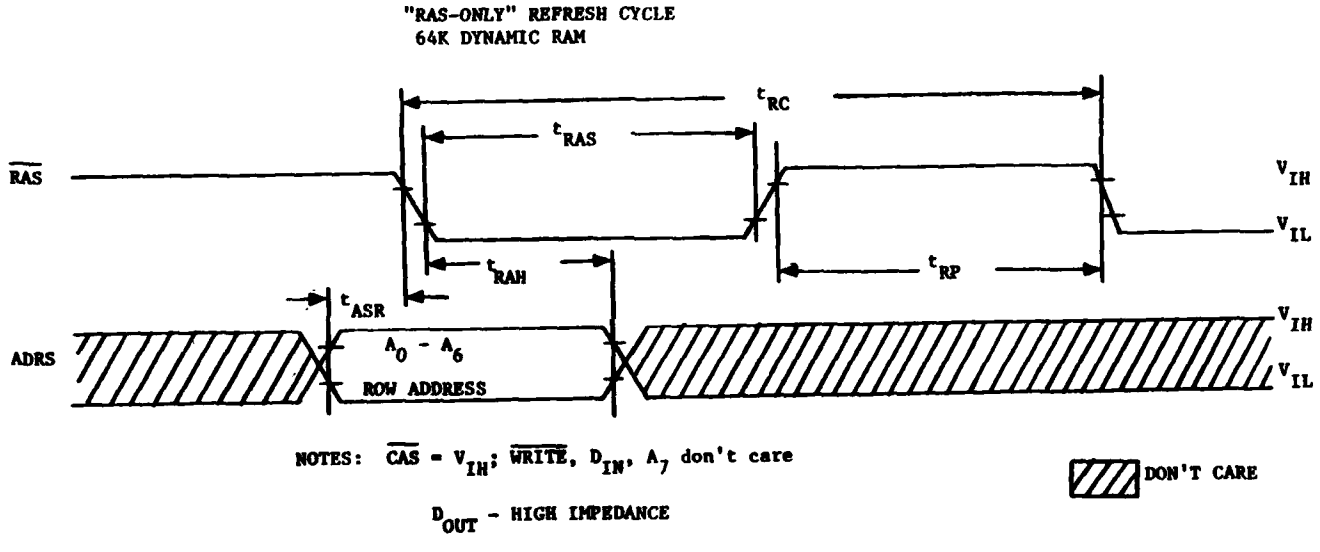


FIGURE 7. "RAS-ONLY" REFRESH CYCLE WAVEFORMS